SONiX Technology Co., Ltd.

SN8F5869 Series Datasheet

8051-based Microcontroller

SN8F58692

SN8F58682

SN8F58652

SN8F58641

SN8F58631

1 Device Overview

1.1 Features

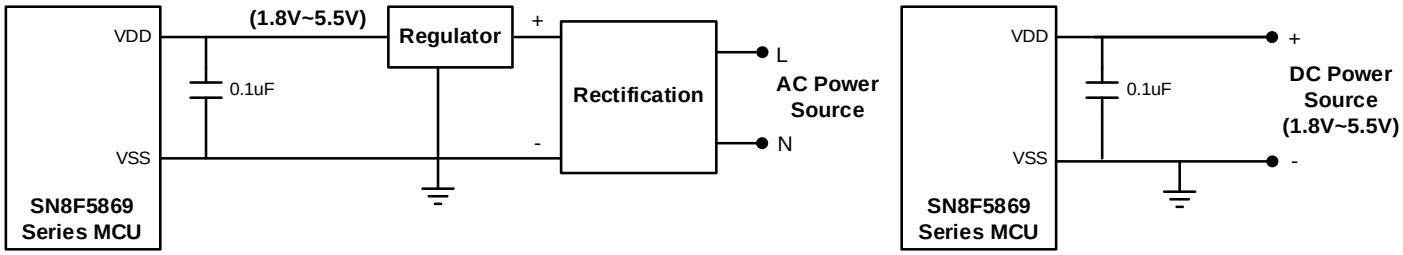
- **Enhanced 8051 microcontroller** with reduced instruction cycle time (up to 12 times 80C51)
- **Up to 24MHz flexible CPU frequency**
  Internal 32 MHz Clock Generator (IHRC)
  1 MHz to 24 MHz crystal
  External synchronous clock source
  Real-time clock with 32.768 kHz crystal
- **Memory configuration**
  64 KB on-chip Flash memory (IROM)
  5KB on-chip Flash memory (IBROM)
  256 bytes internal RAM (IRAM)
  4096 bytes external RAM (XRAM)
- **25 interrupt sources with priority levels control and unique interrupt vectors**
  21 internal interrupts
  4 external interrupts: INT1/2/3/4
- **2 set of DPTR**
- **5 set Timer**
  2 set 8/16-bit timers with 4 operation modes
  2 set 16-bit timers with auto-reload
  1 set 16-bit Capture timer
- **4 set 16-bit PWM generators**:
  Each PWM generator has 4 output channels with individual duty and inverter function
- **12-bit SAR ADC** with 16 external and 3 internal channels, and 5 internal reference voltages
- **Interface**
  4 set UARTs with individual interrupt vector
  1 set I2C with SMBus Support
  1 set SPI interface
- **4x36/5x35/6x34/8x32 R-C-type LCD Driver** with 1/3 bias and 1/4 bias
- **One channel 2KHz/4KHz buzzer output**
- **On-Chip Debug Support**:
  Single-wire debug interface
  5 hardware breakpoints
  Unlimited software breakpoints
  ROM data security/protection
- **Support for embedded boot loader**
- **Debug interface ON/OFF control**
- **Watchdog and programmable external reset**
- **1.7-4.5V 8 section wide range voltage detector**
- **Wide supply voltage (1.8 V – 5.5 V) and temperature (-40 °C to 105 °C) range**

1.2 Applications

- Home automation
- Touch Key

1.3 Power Noise Immunity

The MCU has high-performance operation with robust reliability characteristics. The power pin is VDD. VDD pin is connect to DC power source from DC-DC inverter or regulator and connects a 0.1uF capacitor to VSS pin (ground). For high power noise immunity, connect the C (0.1uF) as near as possible to VDD pin of micro-controller.

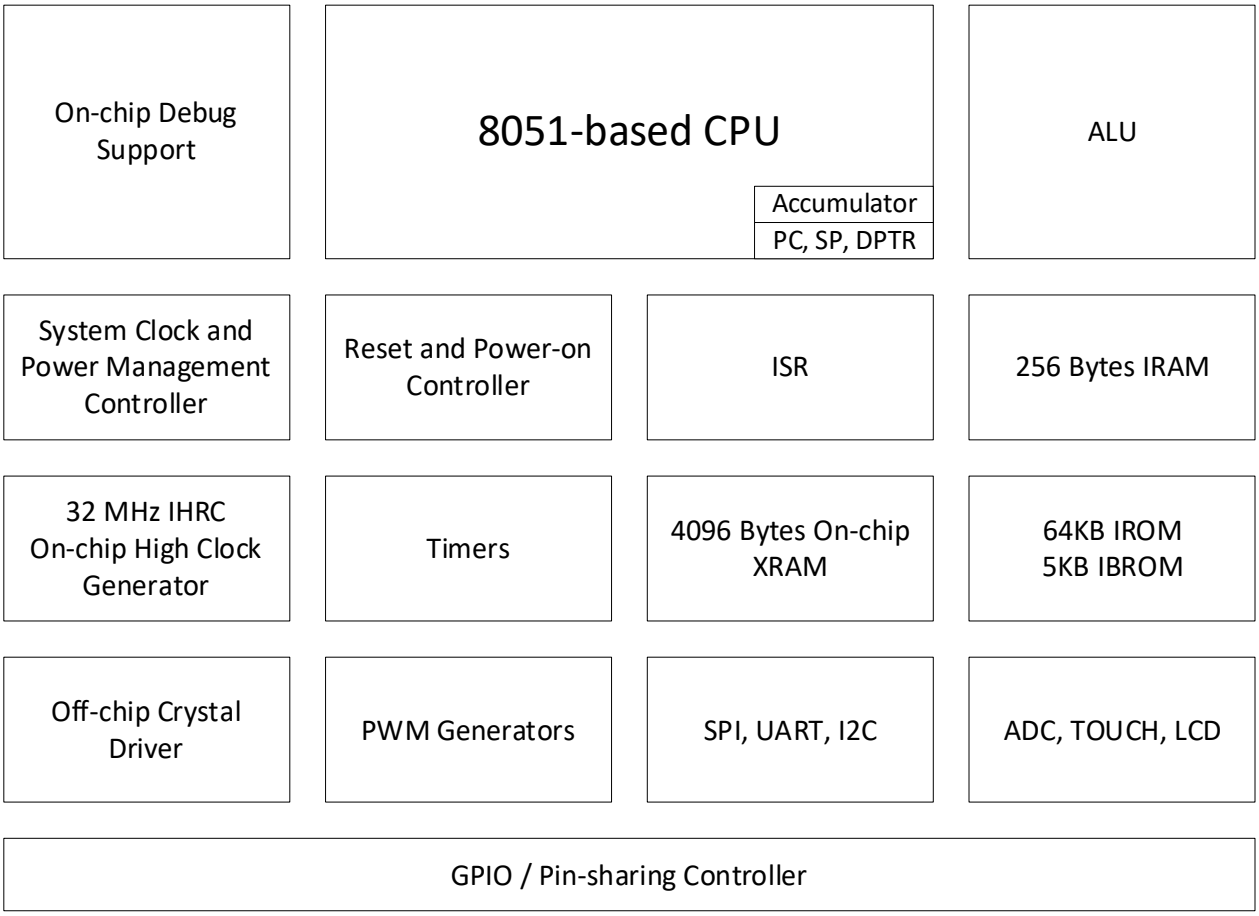


1.4 Features Selection Table

	I/O	PWM Channels	I2C	SPI	UART	ADC ext. Channels	LCD	Touch	Ext. INT	Package Types
SN8F58692	59	15	1	1	4	16	4*36 5*35 6*34 8*32	24	4	LQFP64
SN8F58682	44	13	1	1	4	13	4*25	17	4	LQFP48
SN8F58652	28	6	1	1	3	8	4*14	13	4	LQFP32 QFN32
SN8F58641	25	8	1	1	2	9	-	17	4	SOP28 TSSOP28
SN8F58631	21	6	1	1	2	8	-	13	4	SSOP24

	SN8F5829	SN8F5869
Max. Pin Out	64	64
Max. FCPU Frequency	16MHz	24MHz
IROM	32KB	64KB
IBROM	-	4KB Boot loader 512B Data flash memory 512B Product flash memory
SRAM	256B IRAM 1536KB XRAM	256B IRAM 4096B XRAM
I/O	60	59
16-bit Timer	9	9
PWM	16-ch	15-ch
UART	3	4
SPI	1	1
I2C	1	1
12-bit ADC	16+3	16+3
LCD	R-Type 4*36/5*35/6*34/8*32	R-Type, C-Type 4*36/5*35/6*34/8*32
CRC	-	V
Flash ROM	No need to erase page. Program 1 page (64bytes) 6ms	Erase Page (512 bytes) 4ms

1.5 Block Diagram



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3 Revision History

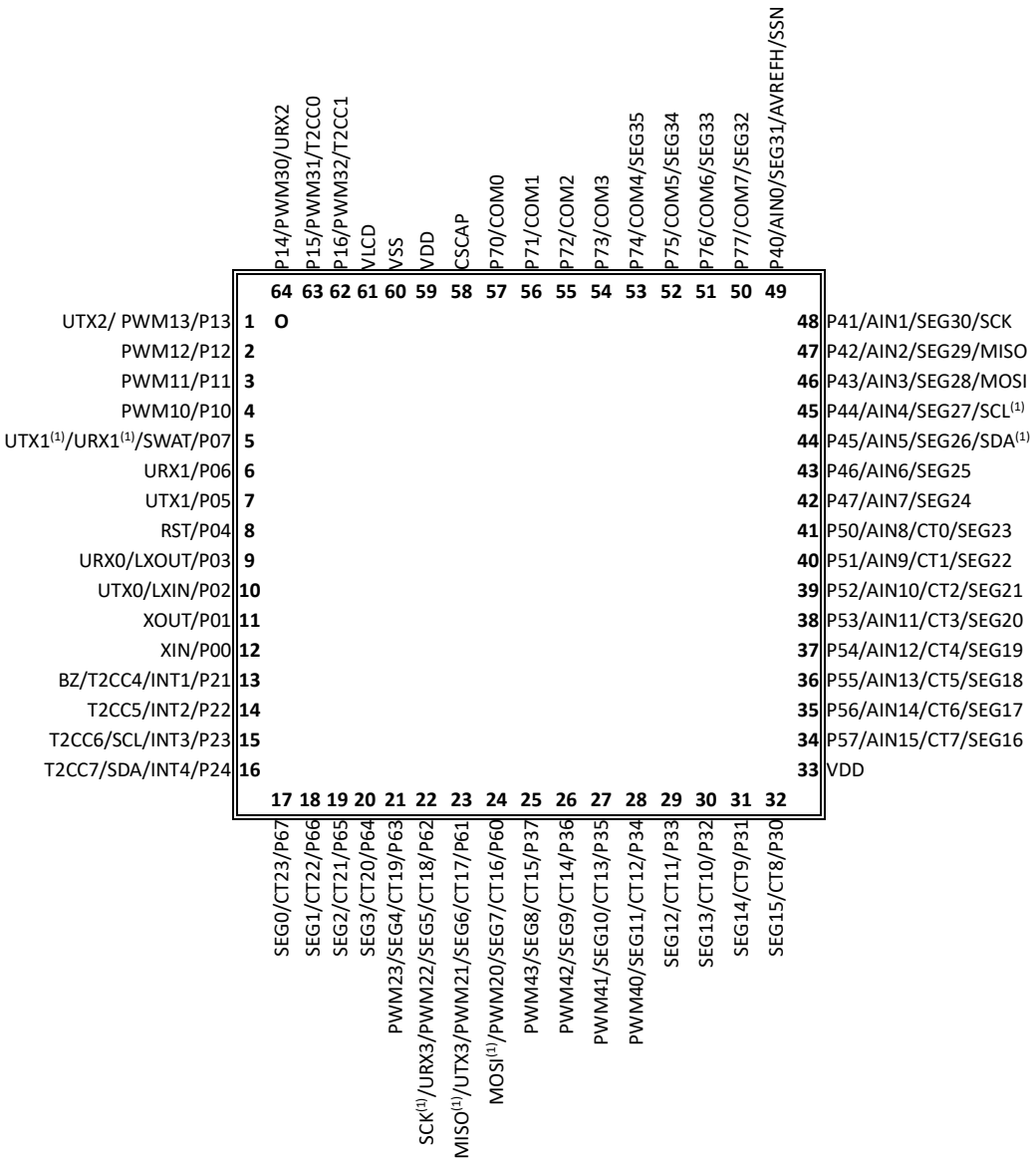
Revision	Date	Description
1.0	Jun. 2024	First issue.
1.1	Jul. 2024	1. Repair an error, omission, etc. 2. Add SOP28, SOP24 pin assignment.
1.2	Aug. 2024	1. Add chapter 29 Single Wire Asynchronous Interface (SWAT). 2. Add erase (512 bytes/page) and program (max 128 bytes/page) information in 27 In-System Program chapter. 3. Add SN8F58692/58641/58631 pin assignment.
1.3	March. 2025	1. Modify typing errors. 2. Modify Features Selection Table. 3. Modify Pin Allocation Table/Pin Descriptions/Pin Characteristic. 4. Modify code option table. 5. Modify system clock timing. 6. Add 21. 2K/4K Buzzer Generator chapter. 7. Modify UART table and update descriptions of UR1MX[1:0]. 8. Modify CRC register description. 9. Update Starter-Kit Circuit. 10. Modify 36. ROM Programming Pin chapter. 11. Modify 37.4 title to QFN32 4x4. 12. Modify PWM duty descriptions and remove PWNnO descriptions. 13. Add 30. ILRC Auto-Calibration chapter. 14. Update 22.4 ADC Converting Time. 15. Update 26.7 LCD Registers. 16. Remove INT0 and T2CC3 related descriptions. 17. Update SPCON register. 18. Update 32. Electrical Characteristics.
1.4	April.2025	1. Update 36.3 MP5 Writer Programming Pin Mapping, and 36.5 SN-Link ISP Programming Pin Mapping. 2. Update 35. SN8F5869 Starter-Kit chapter. 3. Update 32. Electrical Characteristics. 4. Update 37.1 Device Nomenclature. 5. Update 1.3 Features Selection Table. 6. Update 8.1 System Clock and 8.2 High Speed Clock descriptions.
1.5	Jun. 2025	1. Update Starter-Kit schematic and add Power Noise Immunity chapter. 2. Update UART2 register table. 3. Add LCD 1/4 bias and low power mode description.

		4. Update LCD Electrical Characteristics. 5. Add SN8F58631XG package type. 6. Add mapping table to SN8F5829. 7. Remove appendix chapter. 8. Modify typing error. 9. Update Low Speed Clock chapter. 10. Modify Development Environment chapter description. 11. Add Application Circuit chapter.
1.6	Jul. 2025	1. Add IBROM description. 2. Modify security description. 3. Remove SN8F5000 Debug Tool Manual description. 4. Add SSOP24 package information. 5. Modify feature table and MP5 Hardware Connecting. 6. Modify High Speed Clock and Low Speed Clock chapter.
1.7	Aug. 2025	1. Update pin assignment. 2. Add SN8F58641TG package type. 3. Update features selection table.

4 Pin Assignments

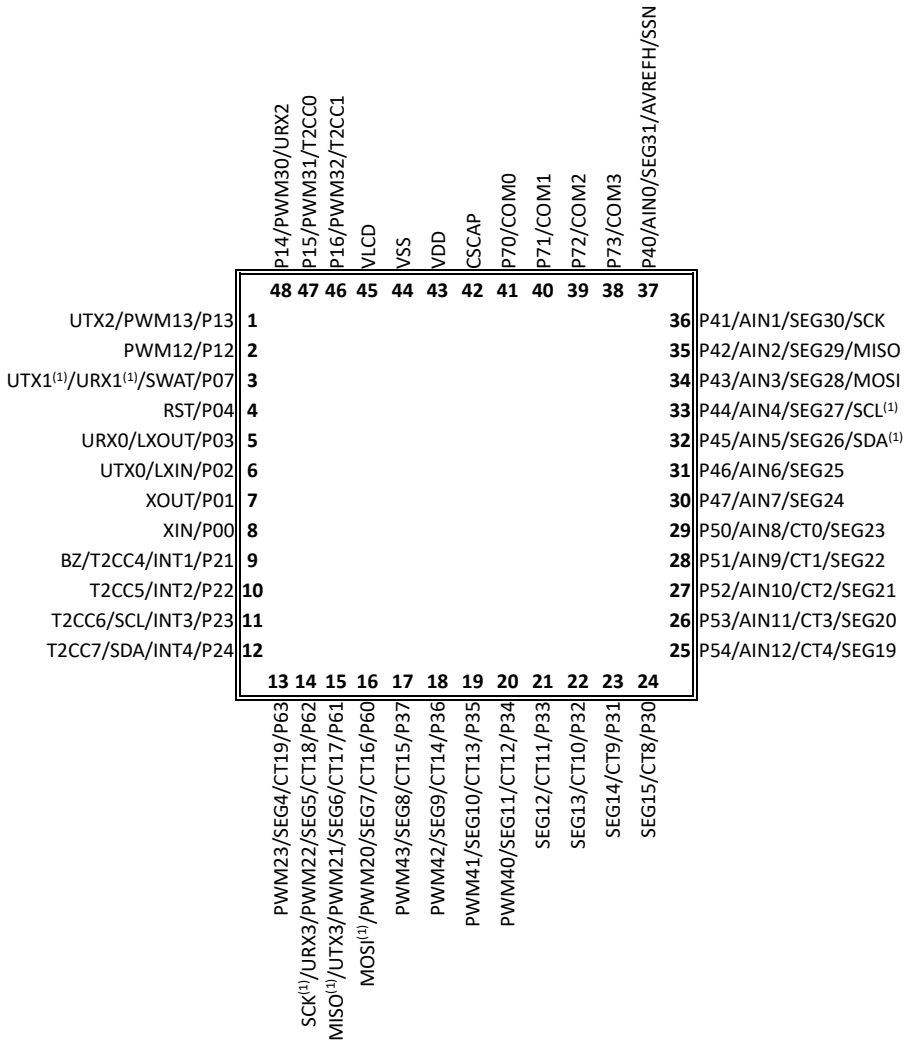
4.1 Pin Diagrams

- SN8F58692F (LQFP64)



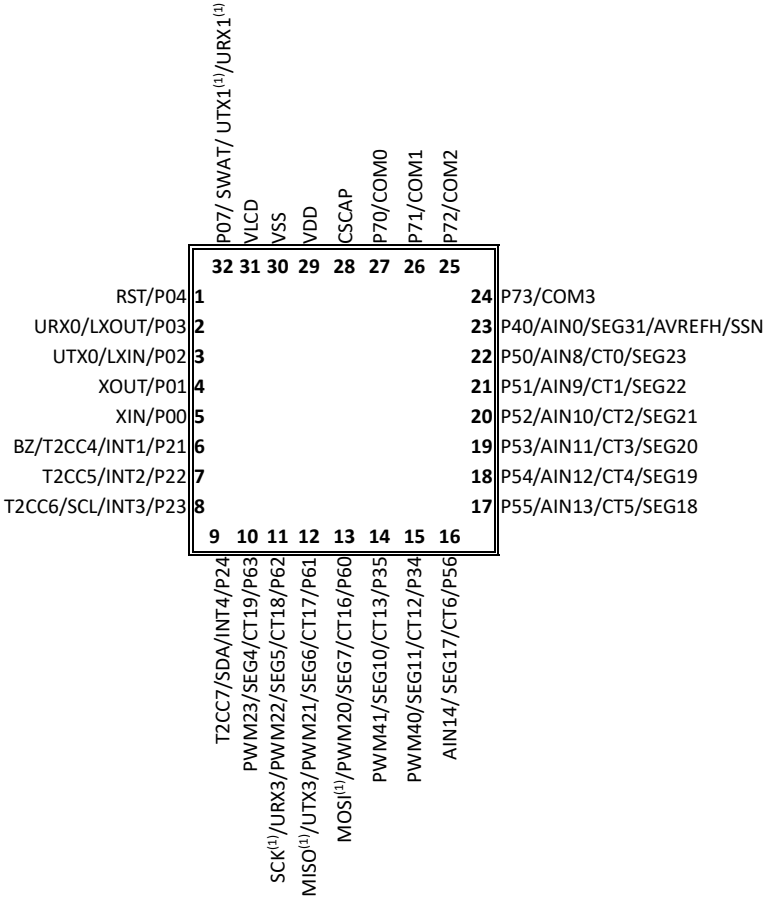
> ✸ ***Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.***
>
> ✸ ***Note: P1.7 and P2.0 are not pin-out and are reserved for internal testing. Strongly recommended to set these pins as input pull-up.***

- SN8F58682F (LQFP48)



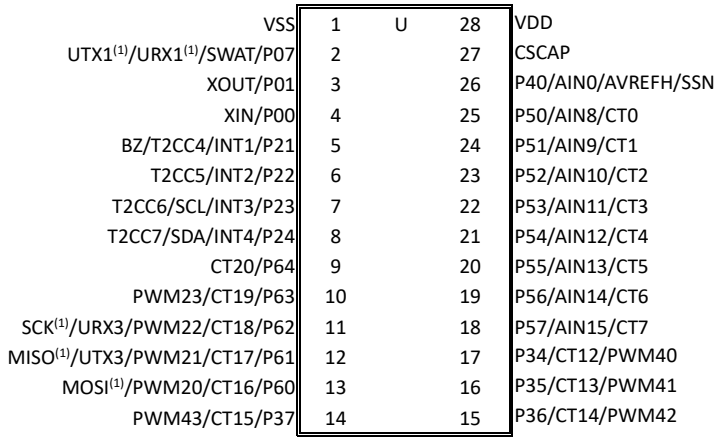
> ✸ ***Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.***
>
> ✸ ***Note: P1.7 and P2.0 are not pin-out and are reserved for internal testing. Strongly recommended to set these pins as input pull-up.***

- SN8F58652F/J (LQFP32/QFN32)



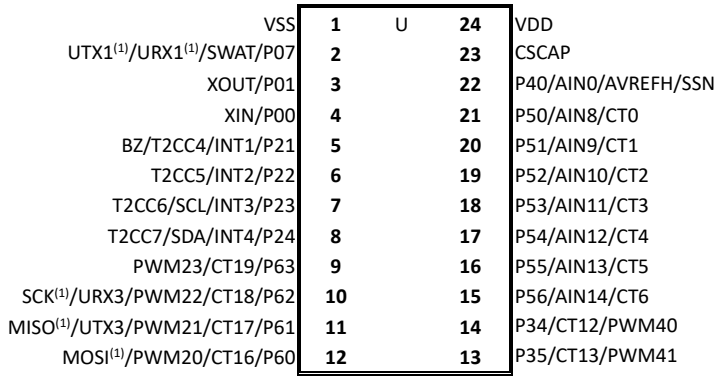
- ***Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.***
- ***Note: P1.7 and P2.0 are not pin-out and are reserved for internal testing. Strongly recommended to set these pins as input pull-up.***

- SN8F58641S/T (SOP28/TSSOP28)



- ***Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.***
- ***Note: P1.7 and P2.0 are not pin-out and are reserved for internal testing. Strongly recommended to set these pins as input pull-up.***

- SN8F58631X (SSOP24)



- ***Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.***
- ***Note: P1.7 and P2.0 are not pin-out and are reserved for internal testing. Strongly recommended to set these pins as input pull-up.***

4.2 Pin Allocation Table

- SN8F58692F (LQFP64)

Port	Open-Drain	Wakeup	External Interrupt	ADC	ADC External Reference	UART	I2C	SPI	T2	PWM	External Reset	Debug interface
P0.0	-	V	-	-	-	-	-	-	-	-	-	-
P0.1	-	V	-	-	-	-	-	-	-	-	-	-
P0.2	V	V	-	-	-	UTX0	-	-	-	-	-	-
P0.3	V	V	-	-	-	URX0	-	-	-	-	-	-
P0.4	-	V	-	-	-	-	-	-	-	-	RST	-
P0.5	V	V	-	-	-	UTX1	-	-	-	-	-	-
P0.6	V	V	-	-	-	URX1	-	-	-	-	-	-
P0.7	V	V	-	-	-	UTX1(1) URX1(1)	-	-	-	-	-	SWAT
P1.0	-	V	-	-	-	-	-	-	-	PWM10	-	-
P1.1	-	V	-	-	-	-	-	-	-	PWM11	-	-
P1.2	-	V	-	-	-	-	-	-	-	PWM12	-	-
P1.3	V	V	-	-	-	UTX2	-	-	-	PWM13	-	-
P1.4	V	V	-	-	-	URX2	-	-	-	PWM30	-	-
P1.5	-	V	-	-	-	-	-	-	T2CC0	PWM31	-	-
P1.6	-	V	-	-	-	-	-	-	T2CC1	PWM32	-	-
*P1.7	-	-	-	-	-	-	-	-	-	-	-	-
*P2.0	-	-	-	-	-	-	-	-	-	-	-	-
P2.1	-	-	INT1	-	-	-	-	-	T2CC4	-	-	-
P2.2	-	-	INT2	-	-	-	-	-	T2CC5	-	-	-
P2.3	-	-	INT3	-	-	-	SCL	-	T2CC6	-	-	-
P2.4	-	-	INT4	-	-	-	SDA	-	T2CC7	-	-	-
P3.0	-	-	-	-	-	-	-	-	-	-	-	-
P3.1	-	-	-	-	-	-	-	-	-	-	-	-
P3.2	-	-	-	-	-	-	-	-	-	-	-	-
P3.3	-	-	-	-	-	-	-	-	-	-	-	-
P3.4	-	-	-	-	-	-	-	-	-	PWM40	-	-
P3.5	-	-	-	-	-	-	-	-	-	PWM41	-	-
P3.6	-	-	-	-	-	-	-	-	-	PWM42	-	-

P3.7	-	-	-	-	-	-	-	-	-	PWM43	-	-
P4.0	-	-	-	AIN0	AVREFH	-	-	SSN	-	-	-	-
P4.1	V	-	-	AIN1	-	-	-	SCK	-	-	-	-
P4.2	V	-	-	AIN2	-	-	-	MISO	-	-	-	-
P4.3	V	-	-	AIN3	-	-	-	MOSI	-	-	-	-
P4.4	-	-	-	AIN4	-	-	SCL(1)	-	-	-	-	-
P4.5	-	-	-	AIN5	-	-	SDA(1)	-	-	-	-	-
P4.6	-	-	-	AIN6	-	-	-	-	-	-	-	-
P4.7	-	-	-	AIN7	-	-	-	-		-	-	-
P5.0	-	-	-	AIN8	-	-	-	-	-	-	-	-
P5.1	-	-	-	AIN9	-	-	-	-	-	-	-	-
P5.2	-	-	-	AIN10	-	-	-	-	-	-	-	-
P5.3	-	-	-	AIN11	-	-	-	-	-	-	-	-
P5.4	-	-	-	AIN12	-	-	-	-	-	-	-	-
P5.5	-	-	-	AIN13	-	-	-	-	-	-	-	-
P5.6	-	-	-	AIN14	-	-	-	-	-	-	-	-
P5.7	-	-	-	AIN15	-	-	-	-	-	-	-	-
P6.0	V	-	-	-	-	-	-	MOSI(1)	-	PWM20	-	-
P6.1	V	-	-	-	-	UTX3	-	MISO(1)	-	PWM21	-	-
P6.2	V	-	-	-	-	URX3	-	SCK(1)	-	PWM22	-	-
P6.3	-	-	-	-	-	-	-	-	-	PWM23	-	-
P6.4	-	-	-	-	-	-	-	-	-	-	-	-
P6.5	-	-	-	-	-	-	-	-	-	-	-	-
P6.6	-	-	-	-	-	-	-	-	-	-	-	-
P6.7	-	-	-	-	-	-	-	-	-	-	-	-
P7.0	-	-	-	-	-	-	-	-	-	-	-	-
P7.1	-	-	-	-	-	-	-	-	-	-	-	-
P7.2	-	-	-	-	-	-	-	-	-	-	-	-
P7.3	-	-	-	-	-	-	-	-	-	-	-	-
P7.4	-	-	-	-	-	-	-	-	-	-	-	-
P7.5	-	-	-	-	-	-	-	-	-	-	-	-
P7.6	-	-	-	-	-	-	-	-	-	-	-	-
P7.7	-	-	-	-	-	-	-	-	-	-	-	-

* P1.7 AND P2.0 are not pin-out and are reserved for internal testing.

4.3 Pin Descriptions

Power Pins

Pin Name	Type	Description
VDD	Power	Power supply
VSS	Power	Ground (0 V)

Port 0

Pin Name	Type	Description
P0.0	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
XIN	Analog Input	System clock: external clock input.
P0.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
XOUT	Analog Output	System clock: drive external crystal/resonator.
P0.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
LXIN	Analog Input	Low clock: external clock input.
UTX0	Digital Output	UART0: transmission pin.
P0.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
LXOUT	Analog Output	Low clock: drive external crystal.
URX0	Digital Input	UART0: reception pin.
P0.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
Reset	Digital Input	System reset (active low).
P0.5	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
UTX1	Digital Output	UART1: transmission pin.
P0.6	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
URX1	Digital Input	UART1: reception pin.
P0.7	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
SWAT	Digital I/O	Debug interface.
UTX1(1)	Digital Output	UART1: transmission pin.
URX1(1)	Digital Input	UART1: reception pin.

Port 1

Pin Name	Type	Description

P1.0	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
PWM10	Digital Output	PWM1: programmable PWM output.
P1.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
PWM11	Digital Output	PWM1: programmable PWM output.
P1.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
PWM12	Digital Output	PWM1: programmable PWM output.
P1.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
PWM13	Digital Output	PWM1: programmable PWM output.
UTX2	Digital Output	UART2: transmission pin.
P1.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
PWM30	Digital Output	PWM3: programmable PWM output.
URX2	Digital input	UART2: reception pin.
P1.5	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
PWM31	Digital Output	PWM3: programmable PWM output.
T2CC0	Digital input	Timer 2: capture 0 input.
P1.6	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
PWM32	Digital Output	PWM3: programmable PWM output.
T2CC1	Digital input	Timer 2: capture 1 input.
P1.7	Digital I/O	GPIO: *Reserved for internal testing.

Port 2

Pin Name	Type	Description
P2.0	Digital I/O	GPIO: *Reserved for internal testing.
P2.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
INT1	Digital Input	INT1: external interrupt 1.
T2CC4	Digital Input	Timer 2: capture 4 input.
BZ	Digital Output	BZ: Buzzer output
P2.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
INT2	Digital Input	INT2: external interrupt 2.
T2CC5	Digital Input	Timer 2: capture 5 input.

P2.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
INT3	Digital Input	INT3: external interrupt 3.
T2CC6	Digital Input	Timer 2: capture 6 input.
SCL	Digital I/O	I2C: clock output (master) or clock input (slave).
P2.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
INT4	Digital Input	INT4: external interrupt 4.
T2CC7	Digital Input	Timer 2: capture 7 input.
SDA	Digital I/O	I2C: data pin.

Port 3

Pin Name	Type	Description
P3.0	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG15	Analog Output	LCD: Segment 15 output.
CT8	Analog Input	CT8: Cap-sensing touch input channel 8.
P3.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG14	Analog Output	LCD: Segment 14 output.
CT9	Analog Input	CT8: Cap-sensing touch input channel 9.
P3.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG13	Analog Output	LCD: Segment 13 output.
CT10	Analog Input	CT8: Cap-sensing touch input channel 10.
P3.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG12	Analog Output	LCD: Segment 12 output.
CT11	Analog Input	CT8: Cap-sensing touch input channel 11.
P3.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM40	Digital Output	PWM4: programmable PWM output.
SEG11	Analog Output	LCD: Segment 11 output.
CT12	Analog Input	CT8: Cap-sensing touch input channel 12.
P3.5	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM41	Digital Output	PWM4: programmable PWM output.
SEG10	Analog Output	LCD: Segment 10 output.
CT13	Analog Input	CT8: Cap-sensing touch input channel 13.

P3.6	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM42	Digital Output	PWM4: programmable PWM output.
SEG9	Analog Output	LCD: Segment 9 output.
CT14	Analog Input	CT8: Cap-sensing touch input channel 14.
P3.7	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM43	Digital Output	PWM4: programmable PWM output.
SEG8	Analog Output	LCD: Segment 8 output.
CT15	Analog Input	CT8: Cap-sensing touch input channel 15.

Port 4

Pin Name	Type	Description
P4.0	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG31	Analog Output	LCD: Segment 31 output.
AIN0	Analog Input	ADC: input channel 0.
AVREFH	Analog Input	ADC: external reference voltage.
SSN	Digital Input	SPI: Slave selection pin.
P4.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG30	Analog Output	LCD: Segment 30 output.
AIN1	Analog Input	ADC: input channel 1.
SCK	Digital I/O	SPI: clock output (master) or clock input (slave).
P4.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG29	Analog Output	LCD: Segment 29 output.
AIN2	Analog Input	ADC: input channel 2.
MISO	Digital I/O	SPI: reception pin (master) or transmission pin (slave).
P4.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG28	Analog Output	LCD: Segment 28 output.
AIN3	Analog Input	ADC: input channel 3.
MOSI	Digital I/O	SPI: transmission pin (master) or reception pin (slave).
P4.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG27	Analog Output	LCD: Segment 27 output.
AIN4	Analog Input	ADC: input channel 4.
SCL(1)	Digital Output	I2C: clock output (master) or clock input (slave).

P4.5	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG26	Analog Output	LCD: Segment 26 output.
AIN5	Analog Input	ADC: input channel 5.
SDA(1)	Digital Output	I2C: data pin.
P4.6	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG25	Analog Output	LCD: Segment 25 output.
AIN6	Analog Input	ADC: input channel 6.
P4.7	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG24	Analog Output	LCD: Segment 24 output.
AIN7	Analog Input	ADC: input channel 7.

Port 5

Pin Name	Type	Description
P5.0	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG23	Analog Output	LCD: Segment 23 output.
AIN8	Analog Input	ADC: input channel 8.
CT0	Analog Input	CT0: Cap-sensing touch input channel 0.
P5.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG22	Analog Output	LCD: Segment 22 output.
AIN9	Analog Input	ADC: input channel 9.
CT1	Analog Input	CT1: Cap-sensing touch input channel 1.
P5.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG21	Analog Output	LCD: Segment 21 output.
AIN10	Analog Input	ADC: input channel 10.
CT2	Analog Input	CT2: Cap-sensing touch input channel 2.
P5.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG20	Analog Output	LCD: Segment 20 output.
AIN11	Analog Input	ADC: input channel 11.
CT3	Analog Input	CT3: Cap-sensing touch input channel 3.
P5.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG19	Analog Output	LCD: Segment 19 output.

AIN12	Analog Input	ADC: input channel 12.
CT4	Analog Input	CT4: Cap-sensing touch input channel 4.
P5.5	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG18	Analog Output	LCD: Segment 18 output.
AIN13	Analog Input	ADC: input channel 13.
CT5	Analog Input	CT5: Cap-sensing touch input channel 5.
P5.6	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG17	Analog Output	LCD: Segment 17 output.
AIN14	Analog Input	ADC: input channel 14.
CT6	Analog Input	CT6: Cap-sensing touch input channel 6.
P5.7	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG16	Analog Output	LCD: Segment 16 output.
AIN15	Analog Input	ADC: input channel 15.
CT7	Analog Input	CT7: Cap-sensing touch input channel 7.

Port 6

Pin Name	Type	Description
P6.0	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM20	Digital Output	PWM2: programmable PWM output.
SEG7	Analog Output	LCD: Segment 7 output.
CT16	Analog Input	CT16: Cap-sensing touch input channel 16.
MOSI(1)	Digital I/O	SPI: transmission pin (master) or reception pin (slave)
P6.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM21	Digital Output	PWM2: programmable PWM output.
SEG6	Analog Output	LCD: Segment 6 output.
CT17	Analog Input	CT17: Cap-sensing touch input channel 17.
MISO(1)	Digital I/O	SPI: reception pin (master) or transmission pin (slave).
UTX3	Digital Output	UART3: transmission pin.
P6.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM22	Digital Output	PWM2: programmable PWM output.
SEG5	Analog Output	LCD: Segment 5 output.
CT18	Analog Input	CT18: Cap-sensing touch input channel 18.
SCK(1)	Digital I/O	SPI: clock output (master) or clock input (slave).

URX3	Digital Input	UART3: reception pin.
P6.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
PWM23	Digital Output	PWM2: programmable PWM output.
SEG4	Analog Output	LCD: Segment 4 output.
CT19	Analog Input	CT19: Cap-sensing touch input channel 19.
P6.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG3	Analog Output	LCD: Segment 3 output.
CT20	Analog Input	CT20: Cap-sensing touch input channel 20.
P6.5	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG2	Analog Output	LCD: Segment 2 output.
CT21	Analog Input	CT21: Cap-sensing touch input channel 21.
P6.6	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG1	Analog Output	LCD: Segment 1 output.
CT22	Analog Input	CT20: Cap-sensing touch input channel 22.
P6.7	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
SEG0	Analog Output	LCD: Segment 0 output.
CT23	Analog Input	CT20: Cap-sensing touch input channel 23.

Port 7

Pin Name	Type	Description
P7.0	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
COM0	Analog Output	LCD: Common 0 output.
P7.1	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
COM1	Analog Output	LCD: Common 1 output.
P7.2	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
COM2	Analog Output	LCD: Common 2 output.
P7.3	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
COM3	Analog Output	LCD: Common 3 output.
P7.4	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.

COM4	Analog Output	LCD: Common 4 output.
SEG35	Analog Output	LCD: Segment 35 output.
P7.5	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
COM5	Analog Output	LCD: Common 5 output.
SEG34	Analog Output	LCD: Segment 34 output.
P7.6	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
COM6	Analog Output	LCD: Common 6 output.
SEG33	Analog Output	LCD: Segment 33 output.
P7.7	Digital I/O	GPIO: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
COM7	Analog Output	LCD: Common 7 output.
SEG32	Analog Output	LCD: Segment 32 output.

4.4 Pin Characteristic

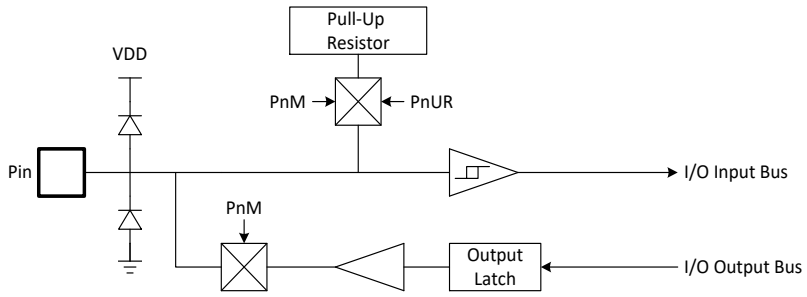
Port	Open-Drain	Sink Current 30mA VSS+0.5V	Drive Current 30mA VSS+0.5V	External Interrupt	Wakeup (Level change)	Shared Pin
P0.0	-	V	V	-	V	XIN
P0.1	-	V	V	-	V	XOUT
P0.2	V	V	V	-	V	LXIN/UTX0
P0.3	V	V	V	-	V	LXOUT/URX0
P0.4	-	V	V	-	V	RST
P0.5	V	V	V	-	V	UTX1
P0.6	V	V	V	-	V	URX1
P0.7	V	V	V	-	V	SWAT/URX0(1)/UTX0(1)
P1.0	-	V	V	-	V	PWM10
P1.1	-	V	V	-	V	PWM11
P1.2	-	V	V	-	V	PWM12
P1.3	V	V	V	-	V	UTX2/PWM13
P1.4	V	V	V	-	V	URX2/PWM30
P1.5	-	V	V	-	V	PWM31/T2CC0
P1.6	-	V	V	-	V	PWM32/T2CC1
*P1.7	-	V	V	-	V	
*P2.0	-	V	V	V	-	
P2.1	-	V	V	V	-	INT1/T2CC4/BZ
P2.2	-	V	V	V	-	INT2/T2CC5
P2.3	-	V	V	V	-	INT3/T2CC6/SCL
P2.4	-	V	V	V	-	INT4/T2CC7/SDA
P3.0	-	V	V	-	-	SEG15/CT8
P3.1	-	V	V	-	-	SEG14/CT9
P3.2	-	V	V	-	-	SEG13/CT10
P3.3	-	V	V	-	-	SEG12/CT11
P3.4	-	V	V	-	-	PWM40/SEG11/CT12
P3.5	-	V	V	-	-	PWM41/SEG10/CT13
P3.6	-	V	V	-	-	PWM42/SEG9/CT14
P3.7	-	V	V	-	-	PWM43/SEG8/CT15
P4.0	-	V	V	-	-	SEG31/AIN0/AVREFH/SSN
P4.1	V	V	V	-	-	SEG30/AIN1/SCK
P4.2	V	V	V	-	-	SEG29/AIN2/MISO
P4.3	V	V	V	-	-	SEG28/AIN3/MOSI
P4.4	-	V	V	-	-	SEG27/AIN4/SCL(1)
P4.5	-	V	V	-	-	SEG26/AIN5/SDA(1)
P4.6	-	V	V	-	-	SEG25/AIN6
P4.7	-	V	V	-	-	SEG24/AIN7
P5.0	-	V	V	-	-	SEG23/AIN8/CT0
P5.1	-	V	V	-	-	SEG22/AIN9/CT1
P5.2	-	V	V	-	-	SEG21/AIN10/CT2
P5.3	-	V	V	-	-	SEG20AIN11/CT3
P5.4	-	V	V	-	-	SEG19/AIN12/CT4
P5.5	-	V	V	-	-	SEG18/AIN13/CT5

P5.6	-	V	V	-	-	SEG17/AIN14/CT6
P5.7	-	V	V	-	-	SEG16/AIN15/CT7
P6.0	V	V	V	-	-	PWM20/SEG7/CT16/MOSI(1)
P6.1	V	V	V	-	-	PWM21/SEG6/CT17/UTX3/MISO(1)
P6.2	V	V	V	-	-	PWM22/SEG5/CT18/URX3/SCK(1)
P6.3	-	V	V	-	-	PWM23/SEG4/CT19
P6.4	-	V	V	-	-	SEG3/CT20
P6.5	-	V	V	-	-	SEG2/CT21
P6.6	-	V	V	-	-	SEG1/CT22
P6.7	-	V	V	-	-	SEG0/CT23
P7.0	-	V	V	-	-	COM0
P7.1	-	V	V	-	-	COM1
P7.2	-	V	V	-	-	COM2
P7.3	-	V	V	-	-	COM3
P7.4	-	V	V	-	-	COM4/SEG35
P7.5	-	V	V	-	-	COM5/SEG34
P7.6	-	V	V	-	-	COM6/SEG33
P7.7	-	V	V	-	-	COM7/SEG32

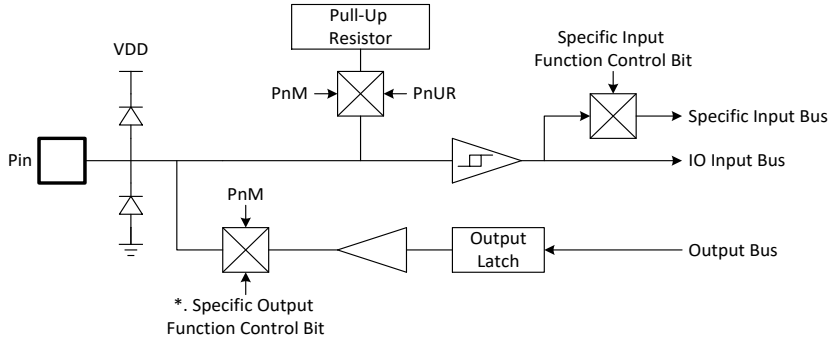
* P1.7 AND P2.0 are not pin-out and are reserved for internal testing.

4.5 Pin Circuit Diagrams

Normal Bi-direction I/O Pin.

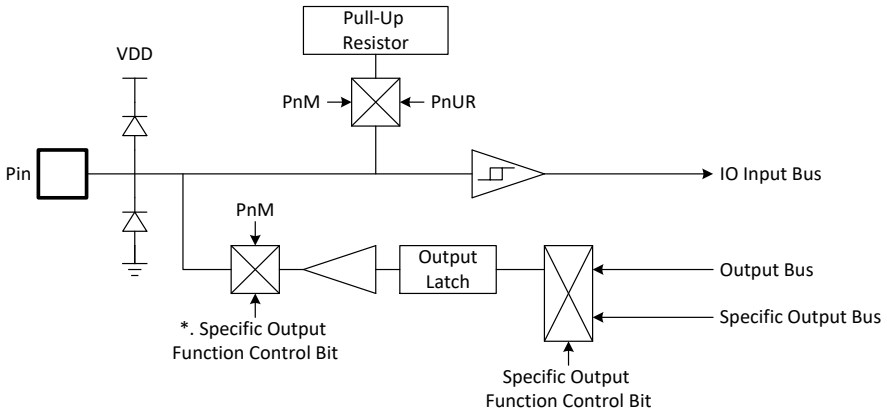


Bi-direction I/O Pin Shared with Specific Digital Input Function, e.g. INT2.



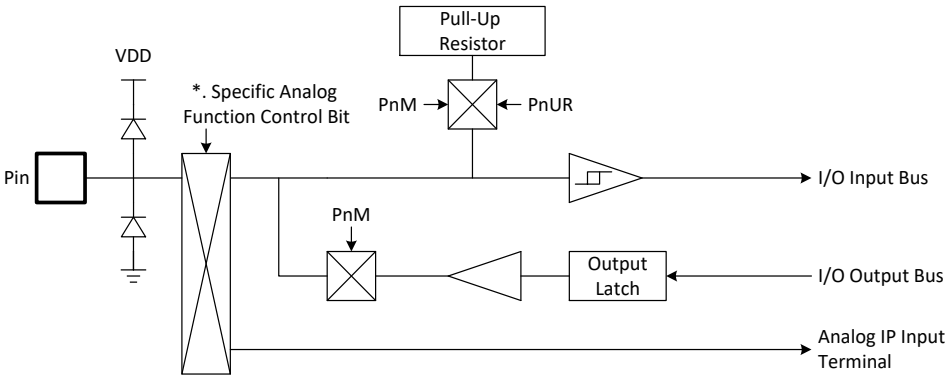
***. Some specific functions switch I/O direction directly, not through PnM register.**

Bi-direction I/O Pin Shared with Specific Digital Output Function, e.g. PWM, UART.



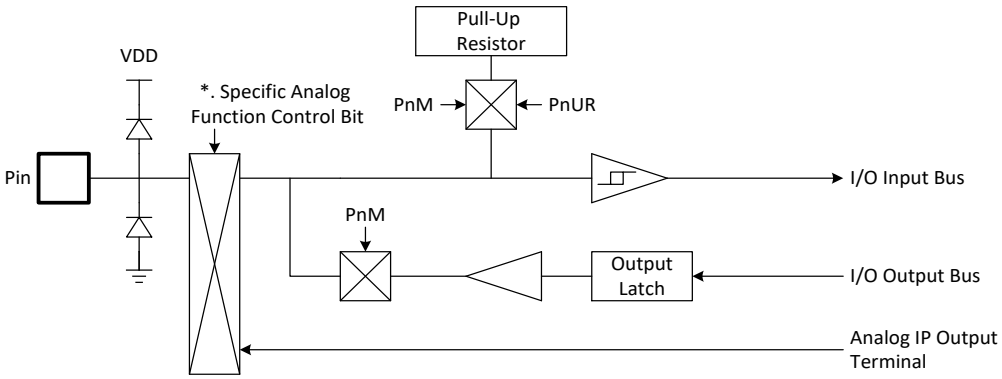
***. Some specific functions switch I/O direction directly, not through PnM register.**

Bi-direction I/O Pin Shared with Specific Analog Input Function, e.g. XIN, ADC.



***. Some specific functions switch I/O direction directly, not through PnM register.**

Bi-direction I/O Pin Shared with Specific Analog Output Function, e.g. XOUT…



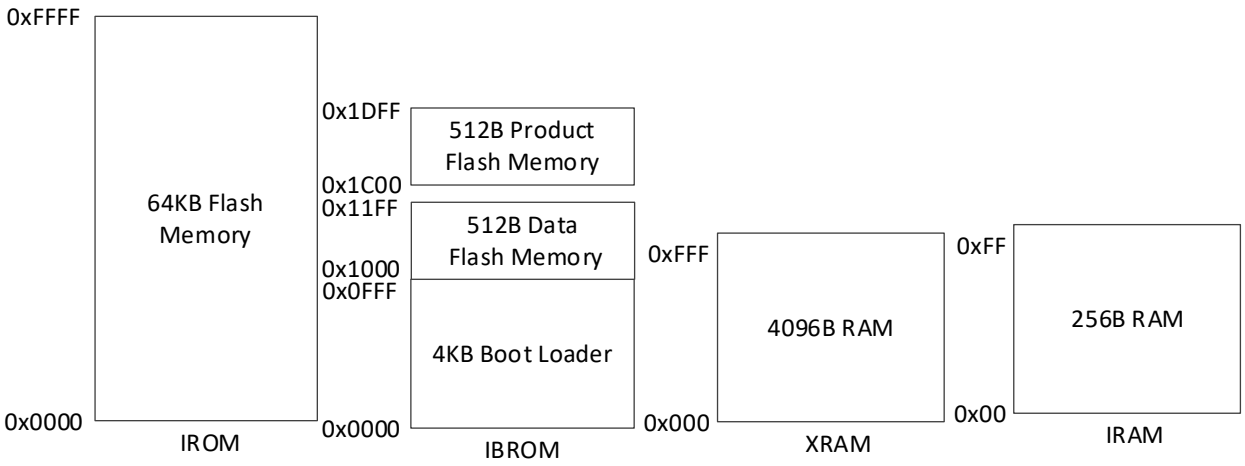
***. Some specific functions switch I/O direction directly, not through PnM register.**

5 CPU

SN8F5000 family is an enhanced 8051 microcontroller (MCU). It is fully compatible with MCS-51 instructions, hence the ability to cooperate with modern development environment (e.g. Keil C51). SN8F5000 CPU has 9.4 to 12.1 times faster than the original 8051 at the same frequency.

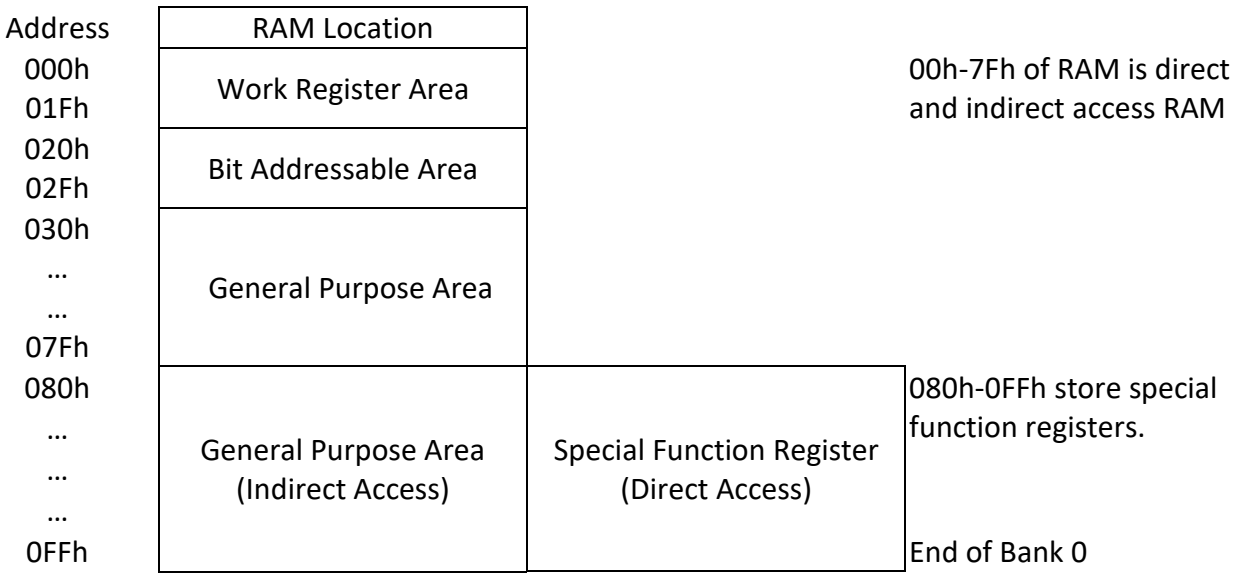
5.1 Memory Organization

SN8F5869 builds in four on-chip memories: internal RAM (IRAM), external RAM (XRAM), program memory (IROM) and information block memory (IBROM). The internal RAM is a 256-byte RAM which has higher access performance (direct and indirect addressing). By contrast, the external RAM has 4096-byte of size, but it requires a longer access period. The program memory is an 64 KB non-volatile memory and has a maximum 24 MHz speed limitation. The information block memory is a 5KB non-volatile memory, including a 4KB boot loader, 512-byte data flash memory and 512-byte product flash memory for device tracking data or series number access.



5.2 Internal RAM (IRAM)

256 X 8-bit RAM (Internal Data Memory)



The 256-byte data RAM in internal data memory is a standard 8051 RAM access configuration. The upper 128-byte RAM is general purpose RAM and can configure by direct addressing access and indirect addressing access. The lower 128-byte can be indirect access RAM in general purpose or direct access RAM in special function register (SFR).

- 0x0000-0x007F: General purpose RAM contains work register area and bit addressable area. In this area, direct or indirect addressing can be used.
- 0x0000-0x001F: Work register area includes 4-bank. Each bank has 8 work registers (R0 - R7) which is selected by RS0/RS1 in PSW register.
- 0x0020-0x002F: Bit addressable area.

In the bit addressable area, user can read or write any single bit in this range by using the unique address for that bit. Supports 16bytes bit addressable RAM area giving 128 addressable bits. Each bit has individual address in the range from 00H to 7FH. Thus, the bit can be addressed directly. Bit0 of the byte 20H has bit address 00H and Bit 7 of the byte 20H has bit address 07H. Bit0 of the byte 2FH has bit address 78H and Bit 7 of the byte 2FH has bit address 7FH. When set “SETB 42H”, it means the bit2 of the byte 28H is set.

Bit Addressable Area	Byte Address	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
	0x20	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
	0x21	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
	0x22	0x10	0x11	0x12	0x13	0x14	0x15	0x16	0x17
	0x23	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
	0x24	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27

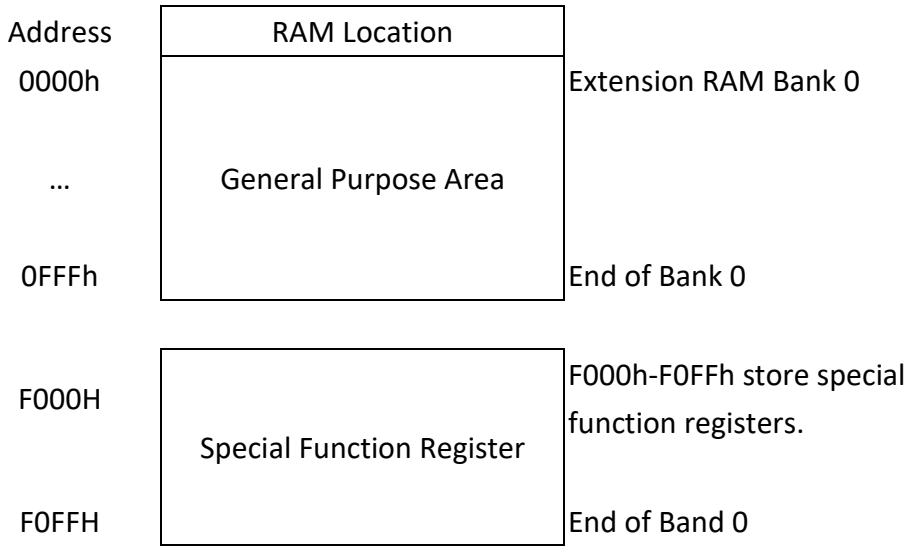
	0x25	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
	0x26	0x30	0x31	0x32	0x33	0x34	0x35	0x36	0x37
	0x27	0x38	0x39	0x3A	0x3B	0x3C	0x3D	0x3E	0x3F
	0x28	0x40	0x41	0x42	0x43	0x44	0x45	0x46	0x47
	0x29	0x48	0x49	0x4A	0x4B	0x4C	0x4D	0x4E	0x4F
	0x2A	0x50	0x51	0x52	0x53	0x54	0x55	0x56	0x57
	0x2B	0x58	0x59	0x5A	0x5B	0x5C	0x5D	0x5E	0x5F
	0x2C	0x60	0x61	0x62	0x63	0x64	0x65	0x66	0x67
	0x2D	0x68	0x69	0x6A	0x6B	0x6C	0x6D	0x6E	0x6F
	0x2E	0x70	0x71	0x72	0x73	0x74	0x75	0x76	0x77
	0x2F	0x78	0x79	0x7A	0x7B	0x7C	0x7D	0x7E	0x7F

- 0x0080~0x00FF: General purpose area in indirect addressing access or special function register in direct addressing access.

5.3 External RAM (XRAM)

4096 X 8-bit XRAM (Extension Data Memory)

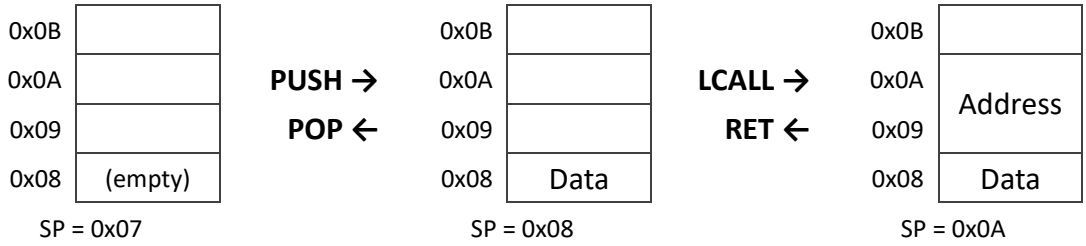
The external RAM enlarges the capacity of variables; it is the lowest access performance in the contrast of internal RAM. Since frequently used variables and local variables are expected to store in internal RAM, the vast majority of external RAM usages are specific. It can be allocated as a variable storage area for lower priority tasks, or look-up table preloaded from ROM to speed up the access period.



The upper 4096-byte XRAM is general purpose RAM and can configure by MOVX instruction access. The lower 256 bytes of XRAM are special function registers (SFRs) that can also be accessed by MOVX instruction.

5.4 Stack

Stack can be assigned to any area of internal RAM (IRAM). However, it requires manual assignment to ensure its area does not overlap other RAM's variables. An overflow or underflow stack could also mistakenly overwrite other RAM's variables; thus, these factors should be considered while arrange the size of stack.



By default, stack pointer (SP register) points to 0x07 which means the stack area begin at IRAM address 0x08. In other word, if a planned stack area is assigned from IRAM address 0xC0, the appropriate SP register is anticipated to set at 0xBF after system reset.

An assembly PUSH instruction costs one byte of stack. LCALL, ACALL instructions and interrupt respectively costs two bytes stack. POP-instruction decreases one count, and a RET/RETI subtract two counts of stack pointer.

5.5 Program Memory (IROM)

The program memory is a non-volatile storage area where stores code, look-up ROM table, and other data with occasional modification. It can be updated by debug tools like SN-Link3, and a program can also self-update via in-system program process (refer to In-system Program).

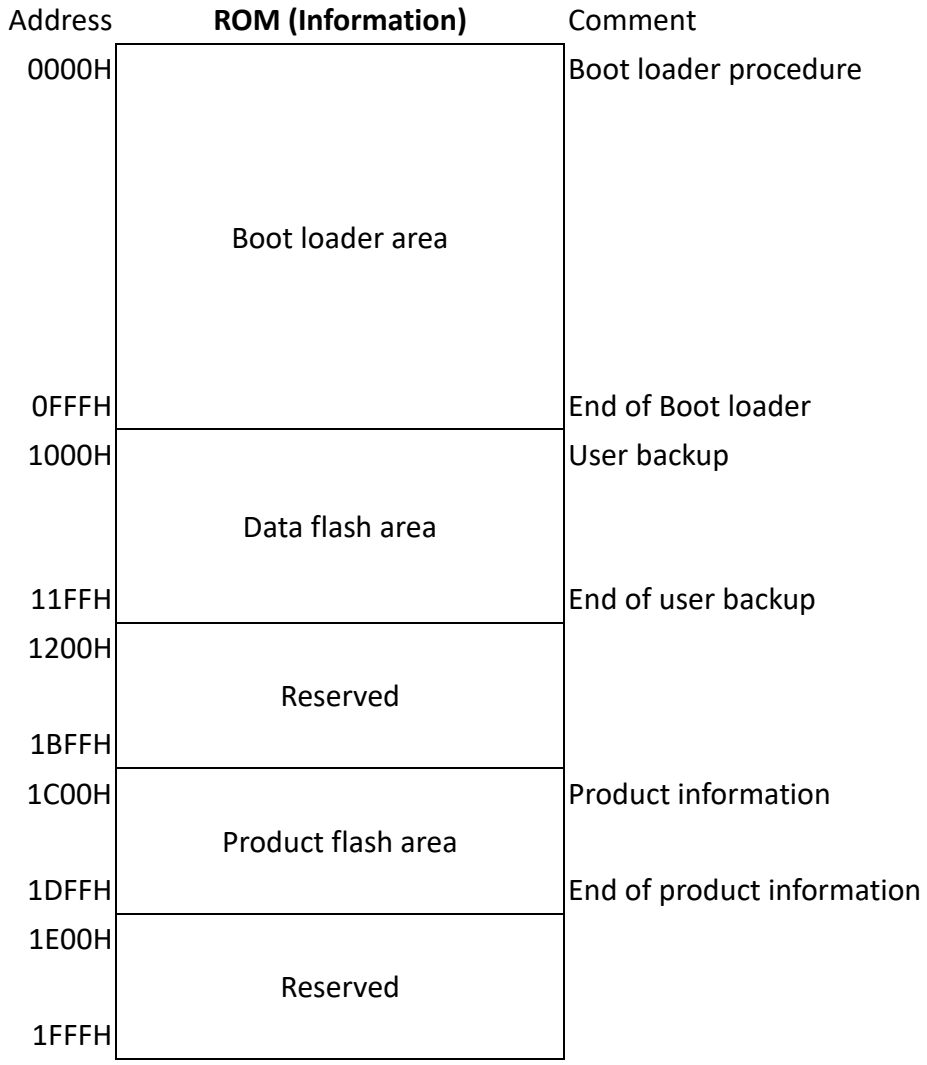
Address	**ROM (Main)**	Comment
0000H	Reset vector	Reset vector
0001H 0002H	General purpose area	User program
0003H	-	**Interrupt vector**
000BH	**TIMER0 Interrupt vector**	
0013H	**INT1 Interrupt vector**	
001BH	**TIMER1 Interrupt vector**	
0023H	**INT2 Interrupt vector**	
002BH	**TIMER2 Interrupt vector**	
0033H	**TIMER3 Interrupt vector**	
003BH	**INT3 Interrupt vector**	
0043H	**I2C Interrupt vector**	
004BH	**SPI Interrupt vector**	
0053H	**UART0 RX Interrupt vector**	
005BH	**UART0 TX Interrupt vector**	

0063H	**UART1 RX Interrupt vector**	
006BH	**UART1 TX Interrupt vector**	
0073H	**TIMER4 Interrupt vector**	
007BH	**INT4 Interrupt vector**	
0083H	**PWM1 Interrupt vector**	
008BH	**PWM2 Interrupt vector**	
0093H	**PWM3 Interrupt vector**	
009BH	**-**	
00A3H	**-**	
00ABH	**ADC Interrupt vector**	
00B3H	**-**	
00BBH	**LVD Interrupt vector**	
00C3H	**UART3 TX Interrupt vector**	
00CBH	**UART3 RX Interrupt vector**	
00D3H	**UART2 TX Interrupt vector**	
00DBH	**UART2 TX Interrupt vector**	
00E3H	**PWM4 TX Interrupt vector**	
00EBH	**-**	
00ECH	General purpose area	User program
.		
.		
.		
.		
.		
.		
.		
.		
FFFFH		End of user program

The main block ROM includes reset vector, Interrupt vector and general purpose area. The reset vector is program beginning address. The interrupt vector is the head of interrupt service routine when any interrupt occurring. The general purpose area is main program area including main loop, sub-routines and data table.

- 0x0000 Reset vector: Program counter points to 0x0000 after any reset events (power on reset, reset pin reset, watchdog reset, LVD reset…).
- 0x0001~0x0002: General purpose area to process system reset operation.
- 0x0003~0x00EB: Multi interrupt vector area. Each of interrupt events has a unique interrupt vector.
- 0x00EC~0xFFFF: General purpose area for user program and ISP (flash function).

5.6 Information Block Memory (IBROM)



The information ROM includes boot loader area, data flash area, product flash area and reserved area. The boot loader procedure is program beginning address. The data flash area is user backup area including data parameter and data record. The product flash area supports user to read device tracking data or series number.

- 0x0000~0x0FFF: Boot loader area support user to on-line update user code.
- 0x1000~0x11FF: Data flash area for user backup data and parameter.
- 0x1C00~0x1C08: Product flash area supports 72 bits Unique ID. Content description is specific information including lot ID, wafer ID and XY-coordinate ID.

Product flash area		
Address	Description	Note
0x1C00	Lot_ID	UID[7:0]
0x1C01	Lot_ID	UID[15:8]
0x1C02	Lot_ID	UID[23:16]
0x1C03	Lot_ID	UID[31:24]

0x1C04	Wafer_ID	UID[39:32]
0x1C05	X-coordinate_ID	UID[47:40]
0x1C06	X-coordinate_ID	UID[55:48]
0x1C07	Y-coordinate_ID	UID[63:56]
0x1C08	Y-coordinate_ID	UID[71:64]

✷ ***Note:***
1. Product flash area address 0x1C09~0x1DFF are reserved area.
2. Before access IBROM by FW (MOVC or ISP), the INFBLK bit must be set to switch memory block to IBROM.
3. If user want to view IBROM data in the Keil memory window, the address of IBROM area must be offset by 0x10000 to identify and switch to IBROM. (ex. Data flash area will be set 0x11000~0x111FF)

5.7 Program Memory Security

The SN8F5869 provides security options at the disposal of the designer to prevent unauthorized access to information stored in FLASH memory. When enable security option, the ROM code is secured and not dumped complete ROM contents. ROM security rule is all address ROM data protected and outputs 0x00.

5.8 Data Pointer

A data pointer helps to specify the XRAM and IROM address while performing MOVX and MOVC instructions. The microcontroller has two set of data pointer (DPH/DPL and DPH1/DPL1) which is selectable by DPS register. The DPC register controls two functions: next DPTR selection and automatically increase/decrease DPTR function.

The next DPTR selection can specify which DPTR is anticipated to use after perform MOVX @DPTR instruction. In other word, the DPS can automatically swap between the two data pointers. To enable this function: write 0 to DPSEL and fill 1 to NDPS firstly, then write 1 to DPSEL and fill 0 to NDPS register.

The automatically increase/decrease DPTR function can make an increment or decrement after perform MOVX @DPTR instruction. As a result, it enables a continuous external RAM access without re-specified DPTR value. Those functions are controlled by the DPC Register, where there are separate DPC register bits for each DPTR, to provide high flexibility in data transfers. The DPC Register address 0x93 points to the window where the actual DPC is selected using the DPS Register, same as for the DPTR.

5.9 Stack and Data Pointer Register

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
DPL	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0
DPH	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0
DPL1	DPL17	DPL16	DPL15	DPL14	DPL13	DPL12	DPL11	DPL10
DPH1	DPH17	DPH16	DPH15	DPH14	DPH13	DPH12	DPH11	DPH10
DPS	-	-	-	-	-	-	-	DPSEL
DPC	-	-	-	-	NDPS	ATMS	ATMD	ATME

SP Register (0x81)

Bit	Field	Type	Initial	Description
7..0	SP	R/W	0x07	Stack pointer

DPL Register (0x82)

Bit	Field	Type	Initial	Description
7..0	DPL[7:0]	R/W	0x00	Low byte of DPTR0

DPH Register (0x83)

Bit	Field	Type	Initial	Description
7..0	DPH[7:0]	R/W	0x00	High byte of DPTR0

DPL1 Register (0x84)

Bit	Field	Type	Initial	Description
7..0	DPL1[7:0]	R/W	0x00	Low byte of DPTR1

DPH1 Register (0x85)

Bit	Field	Type	Initial	Description
7..0	DPH1[7:0]	R/W	0x00	High byte of DPTR1

DPS Register (0x92)

Bit	Field	Type	Initial	Description
7..1	Reserved	R	0x00	
0	DPSEL	R/W	0	DPTR selection 0: DPH/DPL (DPTR0) is selected 1: DPH1/DPL1 (DPTR1) is selected

DPC Register (0x93)

Bit	Field	Type	Initial	Description
7..4	Reserved	R	0x0	
3	NDPS	R/W	0	Next DPTR selection The DPSEL loads this bit automatically after perform any MOVX @DPTR instruction.
2..1	ATMS/ATMD	R/W	00	Automatically increase/decrease DPTR (if ATME applied) 00: +1 after any MOVX @DPTR instruction 01: -1 after any MOVX @DPTR instruction 10: +2 after any MOVX @DPTR instruction 11: -2 after any MOVX @DPTR instruction
0	ATME	R/W	0	Automatically increase/decrease DPTR function 0: Disable 1: Enable

6 Special Function Registers

The SN8F5869 offers many functions that can be controlled via special function registers. Special function registers are placed at both the IRAM address and the XRAM address. The IRAM registers can be accessed by direct addressing, while the XRAM registers are accessed via the MOVX instruction. Register description will be classified according to the addressing range. The 8-bit address refers to the IRAM register and the 16-bit address refers to the XRAM register.

6.1 IRAM Special Function Register Memory Map

BIN / HEX	000	001	010	011	100	101	110	111
F8	P7	P0M	P1M	P2M	P3M	P4M	P5M	PFLAG
F0	B	CRCM	CRCDATL	CRCDATH	SYSMOD	P6M	P7M	SRST
E8	P6	CKSUMCON	CKSUMDATL	CKSUMDATH	IEN3	IRCON3	-	-
E0	ACC	SPSTA	SPCON	SPDAT	-	-	-	LVDCON
D8	P5	BZM	I2CDAT	I2CADR	I2CCON	I2CSTA	SMBSEL	SMBDST
D0	PSW	ADCAL	ADM	ADB	ADR	VREFH	-	-
C8	IEN2	-	-	-	-	-	-	-
C0	P4	DEGCMD	ROMSW	P1W	S3CON	S3BUF	S3RELL	S3RELH
B8	IEN1	IP1	PECMD	PEROML	PEROMH	PERAM	PERAMCNT	PEROMHH
B0	P3	T2M	T2CL	T2CH	CPTM	CPTCL	CPTCH	CPTS
A8	IEN0	IP0	FRQL	FRQH	FRQCMD	LFRQL	LFRQH	CLKCAL
A0	P2	S2CON	S2BUF	S2RELL	S2RELH	IRCON0	-	IRCON2
98	-	S0BUF	S0RELL	S0RELH	S1CON	S1BUF	S1RELL	S1RELH
90	P1	PEDGE1	DPS	DPC	SMODMX	SMODCAL	S0CON2	S0CON
88	TCON	TMOD	TL0	TL1	TH0	TH1	TCON0	PEDGE
80	P0	SP	DPL	DPH	DPL1	DPH1	WDTR	PCON

✷ ***Note: All SFRs in the left-most column are bit-addressable. (Every 0x0/0x8-ending SFR addresses are bit-addressable).***

6.2 IRAM Special Function Register Description

0x80 - 0x9F Registers Description

Register	Address	Description
P0	0x80	Port 0 data buffer.
SP	0x81	Stack pointer register.
DPL	0x82	Data pointer 0 low byte register.
DPH	0x83	Data pointer 0 high byte register.
DPL1	0x84	Data pointer 1 low byte register.
DPH1	0x85	Data pointer 1 high byte register.
WDTR	0x86	Watchdog timer clear register.
PCON	0x87	System mode register.
TCON	0x88	Timer 0 / 1 controls register.
TMOD	0x89	Timer 0 / 1 mode register.
TL0	0x8A	Timer 0 counting low byte register.
TL1	0x8B	Timer 1 counting low byte register.
TH0	0x8C	Timer 0 counting high byte register.
TH1	0x8D	Timer 1 counting high byte register.
TCON0	0x8E	Timer 0 / 1 clock controls register.
PEDGE	0x8F	External interrupt edge controls register.
P1	0x90	Port 1 data buffer.
PEDGE1	0x91	External interrupt edge controls register.
DPS	0x92	Data pointer selects register.
DPC	0x93	Data pointer controls register.
SMODMX	0x94	UART pins selection matrix.
SMODCAL	0x95	UARTs baud rate controls register.
S0CON2	0x96	UARTs baud rate control s register.
S0CON	0x97	UART0 control register.
-	0x98	-
S0BUF	0x99	UART0 data buffer.
S0RELL	0x9A	UART0 reload low byte register.
S0RELH	0x9B	UART0 reload high byte register.
S1CON	0x9C	UART1 control register.
S1BUF	0x9D	UART1 data buffer.
S1RELL	0x9E	UART1 reload low byte register.
S1RELH	0x9F	UART1 reload high byte register.

0xA0 - 0xBF Registers Description

Register	Address	Description
P2	0xA0	Port 2 data buffer.
S2CON	0xA1	UART2 control register.
S2BUF	0xA2	UART2 data buffer.
S2RELL	0xA3	UART2 reload low byte register.
S2RELH	0xA4	UART2 reload high byte register.
IRCON0	0xA5	Interrupts request register.
-	0xA6	-
IRCON2	0xA7	Interrupts request register.
IEN0	0xA8	Interrupts enable register.
IP0	0xA9	Interrupts priority register.
FRQL	0xAA	Clock fine tuning controls buffer low byte.
FRQH	0xAB	Clock fine tuning controls buffer high byte.
FRQCMD	0xAC	Clock fine tuning command register.
LFRQL	0xAD	Low clock fine tuning controls buffer low byte.
LFRQH	0xAE	Low clock fine tuning controls buffer high byte.
CLKCAL	0xAF	ILRC auto-calibration register.
P3	0xB0	Port 3 data buffer.
T2M	0xB1	Timer 2 controls register.
T2CL	0xB2	Timer 2 counting low byte register.
T2CH	0xB3	Timer 2 counting high byte register.
CPTM	0xB4	Capture function of Timer 2 control register.
CPTCL	0xB5	Timer 2 capture buffer low byte.
CPTCH	0xB6	Timer 2 capture buffer high byte.
CPTS	0xB7	Timer 2 capture control register.
IEN1	0xB8	Interrupts enable register.
IP1	0xB9	Interrupts priority register.
PECMD	0xBA	In-System Program command register.
PEROML	0xBB	In-System Program ROM address low byte.
PEROMH	0xBC	In-System Program ROM address high byte.
PERAM	0xBD	In-System Program RAM mapping address.
PERAMCNT	0xBE	ISP Program data length register
PEROMHH	0xBF	ROM access target block register

0xC0 - 0xDF Registers Description

Register	Address	Description
P4	0xC0	Interrupts request register.
DEGCMD	0xC1	Debug mode switch control register
-	0xC2	-
P1W	0xC3	Port 1 wake-up controls register.
S3CON	0xC4	UART3 control register.
S3BUF	0xC5	UART3 data buffer.
S3RELL	0xC6	UART0 reload low byte register.
S3RELH	0xC7	UART0 reload high byte register.
IEN2	0xC8	Interrupts enable register.
-	0xC9	-
-	0xCA	-
-	0xCB	-
-	0xCC	-
-	0xCD	-
-	0xCE	-
-	0xCF	-
PSW	0xD0	System flag register.
ADCAL	0xD1	ADC controls register.
ADM	0xD2	ADC controls register.
ADB	0xD3	ADC data buffer.
ADR	0xD4	ADC resolution selects register.
VREFH	0xD5	ADC reference voltage controls register.
-	0xD6	-
-	0xD7	-
P5	0xD8	Port 5 data buffer.
BZM	0xD9	Buzzer control register.
I2CDAT	0xDA	I2C data buffer.
I2CADR	0xDB	Own I2C slave address.
I2CCON	0xDC	I2C interface operation control register.
I2CSTA	0xDD	I2C Status Code.
SMBSEL	0xDE	SMBus mode controls register.
SMBDST	0xDF	SMBus internal timeout register.

0xE0 - 0xFF Registers Description

Register	Address	Description
ACC	0xE0	Accumulator register.
SPSTA	0xE1	SPI status register.
SPCON	0xE2	SPI control register.
SPDAT	0xE3	SPI data buffer.
-	0xE4	-
-	0xE5	-
-	0xE6	-
LVDCON	0xE7	LVD controls register.
P6	0xE8	Port 6 data buffer.
CKSUMCON	0xE9	Checksum control register.
CKSUMDATL	0xEA	Checksum data low byte register.
CKSUMDATH	0xEB	Checksum data high byte register.
IEN3	0xEC	Interrupts enable register.
IRCON3	0xED	Interrupts request register.
-	0xEE	-
-	0xEF	-
B	0xF0	Multiplication/ division instruction data buffer.
CRCM	0xF1	CRC control register.
CRCDATL	0xF2	CRC data low byte register.
CRCDATH	0xF3	CRC data high byte register.
SYSMOD	0xF4	System controls register.
P6M	0xF5	Port 6 input/output mode register.
P7M	0xF6	Port 7 input/output mode register.
SRST	0xF7	Software reset controls register.
P7	0xF8	Port 7 data buffer.
P0M	0xF9	Port 0 input/output mode register.
P1M	0xFA	Port 1 input/output mode register.
P2M	0xFB	Port 2 input/output mode register.
P3M	0xFC	Port 3 input/output mode register.
P4M	0xFD	Port 4 input/output mode register.
P5M	0xFE	Port 5 input/output mode register.
PFLAG	0xFF	Reset flag register.

6.3 System Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
B	B7	B6	B5	B4	B3	B2	B1	B0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P

ACC Register (0xE0)

Bit	Field	Type	Initial	Description
7..0	ACC[7:0]	R/W	0x00	The ACC is an 8-bit data register responsible for transferring or manipulating data between ALU and data memory. If the result of operating is overflow (OV) or there is carry (C or AC) and parity (P) occurrence, then these flags will be set to PSW register.

B Register (0xF0)

Bit	Field	Type	Initial	Description
7..0	B[7:0]	R/W	0x00	The B register is used during multiplying and division instructions. It can also be used as a scratch-pad register to hold temporary data.

PSW Register (0xD0)

Bit	Field	Type	Initial	Description
7	CY	R/W	0	Carry flag. 0: Addition without carry, subtraction with borrowing signal, rotation with shifting out logic “0”, comparison result < 0. 1: Addition with carry, subtraction without borrowing, rotation with shifting out logic “1”, comparison result ≥ 0.
6	AC	R/W	0	Auxiliary carry flag. 0: If there is no a carry-out from 3rd bit of Accumulator in BCD operations. 1: If there is a carry-out from 3rd bit of Accumulator in BCD operations.
5	F0	R/W	0	General purpose flag 0. General purpose flag available for user.
4..3	RS[1:0]	R/W	00	Register bank select control bit, used to select working register bank. 00: 00H – 07H (Bnak0) 01: 08H – 0FH (Bnak1) 10: 10H – 17H (Bnak2) 11: 18H – 1FH (Bnak3)
2	OV	R/W	0	Overflow flag. 0: Non-overflow in Accumulator during arithmetic Operations. 1: overflow in Accumulator during arithmetic Operations.
1	F1	R/W	0	General purpose flag 1. General purpose flag available for user.
0	P	R	0	Parity flag. Reflects the number of ‘1’s in the Accumulator. 0: if Accumulator contains an even number of ‘1’s. 1: Accumulator contains an odd number of ‘1’s.

6.4 XRAM Special Function Register Memory Map

BIN / HEX	000	001	010	011	100	101	110	111
F0F8	LPSMCH0	LPSMCH1	LPSMCH2	LPSMCH3	LPSMCH4	LPSMCH5	LPSMCH6	LPSMCH7
F0F0	CSC4AVGH	CSC4AVGL	CSC5AVGH	CSC5AVGL	CSC6AVGH	CSC6AVGL	CSC7AVGH	CSC7AVGL
F0E8	CSCAVGH	CSCAVGL	CSC1AVGH	CSC1AVGL	CSC2AVGH	CSC2AVGL	CSC3AVGH	CSC3AVGL
F0E0	CPSTCH0	CPSTCH1	CPSTCH2	-	LPSMCON	-	-	-
F0D8	CSPERD	CSDUTY	TTCON	TTH	TTL	CSDEB	CAPLSCON	CAPLSMOD
F0D0	CSCON	CSCON1	CSCON2	CSCON4	PRSCON	CCAL	CSCH	CSCL
F0C8	-	-	-	-	-	-	-	-
F0C0	-	-	-	-	-	-	-	-
F0B8	-	-	-	-	-	-	-	-
F0B0	-	-	-	-	-	-	-	-
F0A8	PW40DH	PW40DL	PW41DH	PW41DL	PW42DH	PW42DL	PW43DH	PW43DL
F0A0	PW30DH	PW30DL	PW31DH	PW31DL	PW32DH	PW32DL	-	-
F098	PW20DH	PW20DL	PW21DH	PW21DL	PW22DH	PW22DL	PW23DH	PW23DL
F090	PW10DH	PW10DL	PW11DH	PW11DL	PW12DH	PW12DL	PW13DH	PW13DL
F088	PW4M	PW4CH	PW4NV	-	-	-	PW4YH	PW4YL
F080	PW3M	PW3CH	PW3NV	-	-	-	PW3YH	PW3YL
F078	PW2M	PW2CH	PW2NV	-	-	-	PW2YH	PW2YL
F070	PW1M	PW1CH	PW1NV	-	-	-	PW1YH	PW1YL
F068	T4M	T4CH	T4CL	T4RH	T4RL	-	-	-
F060	T3M	T3CH	T3CL	T3RH	T3RL	-	-	-
F058	-	-	-	-	-	-	-	-
F050	-	-	-	-	-	-	-	-
F048	SEG32	SEG33	SEG34	SEG35	-	-	-	-
F040	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31
F038	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23
F030	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
F028	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7
F020	LCDM1	LCDM2	LCDM3	LCDSEGEN0	LCDSEGEN1	LCDSEGEN2	LCDSEGEN3	LCDSEGEN4
F018	ODCON	-	PDRV	-	-	-	-	LCDTEST
F010	P0CON	P1CON	P2CON	P3CON	P4CON	P5CON	P6CON	P7CON
F008	P0DR	P1DR	P2DR	P3DR	P4DR	P5DR	P6DR	P7DR
F000	P0UR	P1UR	P2UR	P3UR	P4UR	P5UR	P6UR	P7UR

✸ ***Note: the XRAM registers are accessed via the MOVX instruction.***

6.5 XRAM Special Function Register Description

0xF000 - 0xF01F Registers Description

Register	Address	Description
P0UR	0xF000	Port0 pull-up controls register.
P1UR	0xF001	Port1 pull-up controls register.
P2UR	0xF002	Port2 pull-up controls register.
P3UR	0xF003	Port3 pull-up controls register.
P4UR	0xF004	Port4 pull-up controls register.
P5UR	0xF005	Port5 pull-up controls register.
P6UR	0xF006	Port6 pull-up controls register.
P7UR	0xF007	Port7 pull-up controls register.
P0DR	0xF008	Port0 pull-down controls register.
P1DR	0xF009	Port1 pull-down controls register.
P2DR	0xF00A	Port2 pull-down controls register.
P3DR	0xF00B	Port3 pull-down controls register.
P4DR	0xF00C	Port4 pull-down controls register.
P5DR	0xF00D	Port5 pull-down controls register.
P6DR	0xF00E	Port6 pull-down controls register.
P7DR	0xF00F	Port7 pull-down controls register.
P0CON	0xF010	Port 0 configuration controls register.
P1CON	0xF011	Port 1 configuration controls register.
P2CON	0xF012	Port 2 configuration controls register.
P3CON	0xF013	Port 3 configuration controls register.
P4CON	0xF014	Port 4 configuration controls register.
P5CON	0xF015	Port 5 configuration controls register.
P6CON	0xF016	Port 6 configuration controls register.
P7CON	0xF017	Port 7 configuration controls register.
ODCON	0xF018	I/O open drain control register.
-	0xF019	-
PDRV	0xF01A	GPIO driving strength control bit.
	0xF01B	
-	0xF01C	-
-	0xF01D	-
-	0xF01E	-
LCDTEST	0xF01F	-

0xF020 - 0xF03F Registers Description

Register	Address	Description
LCDM1	0xF020	LCD control register.
LCDM2	0xF021	LCD control register.
LCDM3	0xF022	LCD control register.
LCDSEGEN0	0xF023	LCD segment enable control register.
LCDSEGEN1	0xF024	LCD segment enable control register.
LCDSEGEN2	0xF025	LCD segment enable control register.
LCDSEGEN3	0xF026	LCD segment enable control register.
LCDSEGEN4	0xF027	LCD segment enable control register.
SEG0	0xF028	LCD data buffer.
SEG1	0xF029	LCD data buffer.
SEG2	0xF02A	LCD data buffer.
SEG3	0xF02B	LCD data buffer.
SEG4	0xF02C	LCD data buffer.
SEG5	0xF02D	LCD data buffer.
SEG6	0xF02E	LCD data buffer.
SEG7	0xF02F	LCD data buffer.
SEG8	0xF030	LCD data buffer.
SEG9	0xF031	LCD data buffer.
SEG10	0xF032	LCD data buffer.
SEG11	0xF033	LCD data buffer.
SEG12	0xF034	LCD data buffer.
SEG13	0xF035	LCD data buffer.
SEG14	0xF036	LCD data buffer.
SEG15	0xF037	LCD data buffer.
SEG16	0xF038	LCD data buffer.
SEG17	0xF039	LCD data buffer.
SEG18	0xF03A	LCD data buffer.
SEG19	0xF03B	LCD data buffer.
SEG20	0xF03C	LCD data buffer.
SEG21	0xF03D	LCD data buffer.
SEG22	0xF03E	LCD data buffer.
SEG23	0xF03F	LCD data buffer.

0xF40 - 0xF05F Registers Description

Register	Address	Description
SEG24	0xF040	LCD data buffer.
SEG25	0xF041	LCD data buffer.
SEG26	0xF042	LCD data buffer.
SEG27	0xF043	LCD data buffer.
SEG28	0xF044	LCD data buffer.
SEG29	0xF045	LCD data buffer.
SEG30	0xF046	LCD data buffer.
SEG31	0xF047	LCD data buffer.
SEG32	0xF048	LCD data buffer.
SEG33	0xF049	LCD data buffer.
SEG34	0xF04A	LCD data buffer.
SEG35	0xF04B	LCD data buffer.
-	0xF04C	-
-	0xF04D	-
-	0xF04E	-
-	0xF04F	-
-	0xF050	-
-	0xF051	-
-	0xF052	-
-	0xF053	-
-	0xF054	-
-	0xF055	-
-	0xF056	-
-	0xF057	-
-	0xF058	-
-	0xF059	-
-	0xF05A	-
-	0xF05B	-
-	0xF05C	-
-	0xF05D	-
-	0xF05E	-
-	0xF05F	-

0xF60 - 0xF07F Registers Description

Register	Address	Description
T3M	0xF060	Timer 3 controls register.
T3CH	0xF061	Timer 3 counting high byte register.
T3CL	0xF062	Timer 3 counting low byte register.
T3RH	0xF063	Timer 3 cycle controls buffer high byte
T3RL	0xF064	Timer 3 cycle controls buffer low byte.
-	0xF065	-
-	0xF066	-
-	0xF067	-
T4M	0xF068	Timer 4 controls register.
T4CH	0xF069	Timer 4 counting high byte register.
T4CL	0xF06A	Timer 4 counting low byte register.
T4RH	0xF06B	Timer 4 cycle controls buffer high byte.
T4RL	0xF06C	Timer 4 cycle controls buffer low byte.
-	0xF06D	-
-	0xF06E	-
-	0xF06F	-
PW1M	0xF070	PWM1 controls register.
PW1CH	0xF071	PWM1 channels control register.
PW1NV	0xF072	PWM1 output inverse control register.
-	0xF073	
-	0xF074	-
-	0xF075	-
PW1YH	0xF076	PWM1 cycle controls buffer high byte.
PW1YL	0xF077	PWM1 cycle controls buffer low byte.
PW2M	0xF078	PWM2 controls register.
PW2CH	0xF079	PWM2 channels control register.
PW2NV	0xF07A	PWM2 output inverse control register.
-	0xF07B	-
-	0xF07C	-
-	0xF07D	-
PW2YH	0xF07E	PWM2 cycle controls buffer high byte.
PW2YL	0xF07F	PWM2 cycle controls buffer low byte.

0xF80 - 0xF09F Registers Description

Register	Address	Description
PW3M	0xF080	PWM3 controls register.
PW3CH	0xF081	PWM3 channels control register.
PW3NV	0xF082	PWM3 output inverse control register.
-	0xF083	-
-	0xF084	-
-	0xF085	-
PW3YH	0xF086	PWM3 cycle controls buffer high byte.
PW3YL	0xF087	PWM3 cycle controls buffer low byte.
PW4M	0xF088	PWM4 controls register.
PW4CH	0xF089	PWM4 channels control register.
PW4NV	0xF08A	PWM4 output inverse control register.
-	0xF08B	
-	0xF08C	-
-	0xF08D	-
PW4YH	0xF08E	PWM4 cycle controls buffer high byte.
PW4YL	0xF08F	PWM4 cycle controls buffer low byte.
PW10DH	0xF090	PWM10 duty controls buffer high byte.
PW10DL	0xF091	PWM10 duty controls buffer low byte.
PW11DH	0xF092	PWM11 duty controls buffer high byte.
PW11DL	0xF093	PWM11 duty controls buffer low byte.
PW12DH	0xF094	PWM12 duty controls buffer high byte.
PW12DL	0xF095	PWM12 duty controls buffer low byte.
PW13DH	0xF096	PWM13 duty controls buffer high byte.
PW13DL	0xF097	PWM13 duty controls buffer low byte.
PW20DH	0xF098	PWM20 duty controls buffer high byte.
PW20DL	0xF099	PWM20 duty controls buffer low byte.
PW21DH	0xF09A	PWM21 duty controls buffer high byte.
PW21DL	0xF09B	PWM21 duty controls buffer low byte.
PW22DH	0xF09C	PWM22 duty controls buffer high byte.
PW22DL	0xF09D	PWM22 duty controls buffer low byte.
PW23DH	0xF09E	PWM23 duty controls buffer high byte.
PW23DL	0xF09F	PWM23 duty controls buffer low byte.

0xF0A0 - 0xF0BF Registers Description

Register	Address	Description
PW30DH	0xF0A0	PWM30 duty controls buffer high byte.
PW30DL	0xF0A1	PWM30 duty controls buffer low byte.
PW31DH	0xF0A2	PWM31 duty controls buffer high byte.
PW31DL	0xF0A3	PWM31 duty controls buffer low byte.
PW32DH	0xF0A4	PWM32 duty controls buffer high byte.
PW32DL	0xF0A5	PWM32 duty controls buffer low byte.
-	0xF0A6	-
-	0xF0A7	-
PW40DH	0xF0A8	PWM40 duty controls buffer high byte.
PW40DL	0xF0A9	PWM40 duty controls buffer low byte.
PW41DH	0xF0AA	PWM41 duty controls buffer high byte.
PW41DL	0xF0AB	PWM41 duty controls buffer low byte.
PW42DH	0xF0AC	PWM42 duty controls buffer high byte.
PW42DL	0xF0AD	PWM42 duty controls buffer low byte.
PW43DH	0xF0AE	PWM43 duty controls buffer high byte.
PW43DL	0xF0AF	PWM43 duty controls buffer low byte.
-	0xF0B0	-
-	0xF0B1	-
-	0xF0B2	-
-	0xF0B3	-
-	0xF0B4	-
-	0xF0B5	-
-	0xF0B6	-
-	0xF0B7	-
-	0xF0B8	-
-	0xF0B9	-
-	0xF0BA	-
-	0xF0BB	-
-	0xF0BC	-
-	0xF0BD	-
-	0xF0BE	-
-	0xF0BF	-

6.6 Register Declaration

SN8F5869 has many registers to control various functions, but SFR name is not predefined in the C51 / A51 compiler. To make programming easier and therefore need to add header files to declare SFR name.

When using the assembly code programs, please add the following sentence.

```
$NOMOD51 ; Do not recognize the 8051-specific predefined special register.
#define __XRAM_SFR_H__ ; For XRAM Register Declaration.
#include <SN8F5869.H>
```

When using the C code programs, please add the following sentence.

```
#define __XRAM_SFR_H__ // For XRAM Register Declaration.
#include <SN8F5869.H>
```

After adding the header file, user can use name of registers to program. During compilation, the compiler will register name translate into register position through the header file.

Different devices need to use a different header file to declare, but the option file is to use the same.

Device	Header file	Options file
SN8F5869	SN8F5869.h	OPTIONS_SN8F5869.A51
SN8F5868	SN8F5868.h	OPTIONS_SN8F5869.A51
SN8F5865	SN8F5865.h	OPTIONS_SN8F5869.A51
SN8F5864	SN8F5864.h	OPTIONS_SN8F5869.A51
SN8F5863	SN8F5863.h	OPTIONS_SN8F5869.A51

✷ ***Note:***

1. The XRAM registers are declared in the main program file and are available for all program files.

2. The XRAM registers are declared only in the main program to avoid duplicate declarations. Therefore, "# define _XRAM_SFR_H_" word string do not add to other program files, to avoid compilation errors.

3. Before including the header file, you must define the "_XRAM_SFR_H_" word string to avoid compilation errors.

6.7 XRAM Register Description

Although the XRAM register is accessed through the MOVX instruction, it is also possible to program code with the SFR name without referencing the address.

When using the assembly code program, you can refer to the following method.

```
MOV     DPTR, #PW1M
MOV     A, #08H
MOVX    @DPTR, A

MOV     DPTR, #P0UR
MOVX    A, @DPTR
MOV     TMP, A ; TMP is direct addressing variable
```

When using the C code program, you can refer to the following method.

```
PW1M = 0x08;
TMP = P0UR; // TMP is direct addressing variable
```

When using assembly code, there is another way to write code faster. The header file has two macros to provide quick and easy programming.

```
WRXSFR  XRAM register, direct addressing variable (or register, #data)
RDXSFR  direct addressing variable (or register), XRAM register
```

Example:

```
WRXSFR  PW1M, #08H
WRXSFR  P1UR, B
WRXSFR  PW2YH, TMP ; TMP is direct addressing variable

RDXSFR  B, PW1M
RDXSFR  TMP, P0UR ; TMP is direct addressing variable
```

✸ ***Note:***

1. Using macro does not increase the speed of instructions, but simplifies the program code.

2. The macro is already included in the header file and can be used directly.

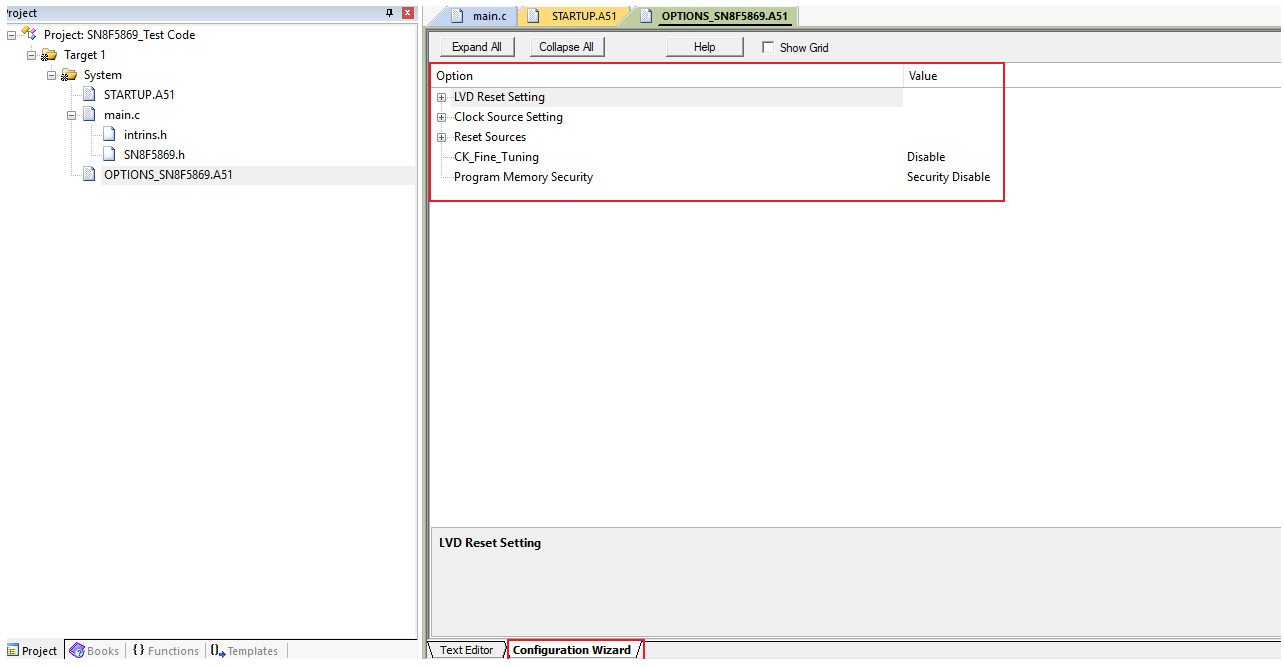
7 Reset and Power-on Controller

The reset and power-on controller has four reset sources: low voltage detectors (LVDs), watchdog, programmable external reset pin, and software reset. The first three sources would trigger an additional power-on sequence. Subsequently, the microcontroller initializes all registers and starts program execution with its reset vector (ROM address 0x0000).

7.1 Configuration of Reset and Power-on Controller

SONiX publishes a *SN8F5869_OPTIONS.A51 file* in *SN-Link Driver for Keil C51.exe* (downloadable on cooperative website: www.sonix.com.tw). This *options file* contains appropriate parameters of reset sources and CPU clock source selection, and is strongly recommended to add to Keil project. The option items are as following:

- LVD Reset Setting
- Program Memory Security
- CPU Clock Source
- CK_Fine_Tuning
- Reset Source : External Reset / GPIO Shared Pin
- Reset Source : Watchdog Reset & Overflow Period



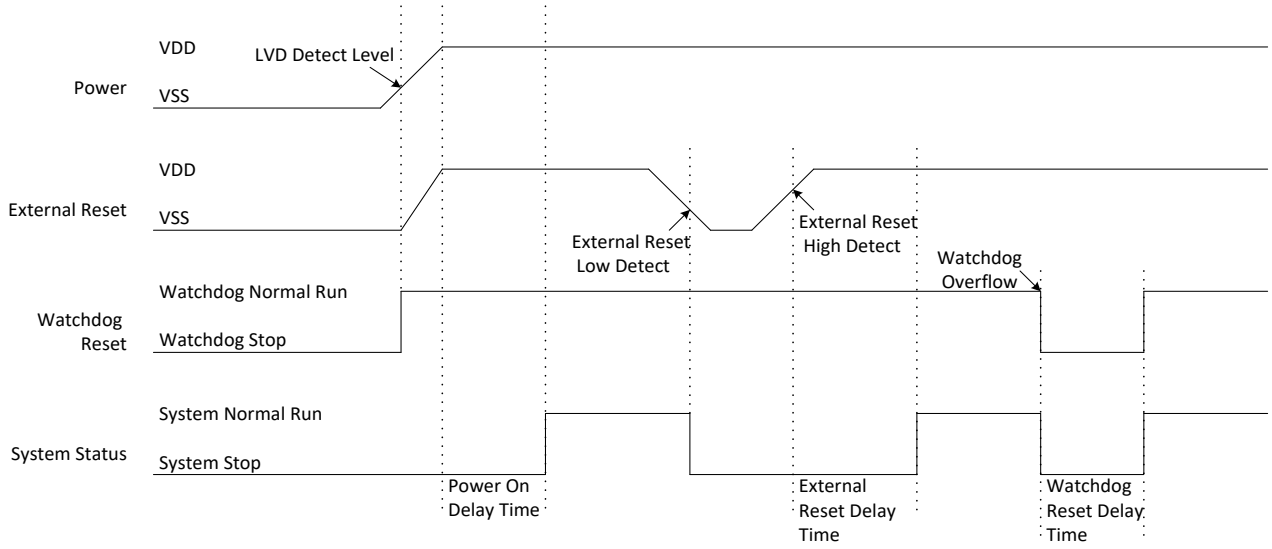
The code option is the system hardware configurations including oscillator type, watchdog timer operation, LVD option, reset pin option and flash ROM security control. The code option items are as following table:

Code Option	Content	Function Description
Program Memory Security	Security Disable	All address ROM data can be accessed.
	Security Enable	All address ROM data are protected. When security level from enable to disable, Mass Erase User ROM.
CPU Clock Source	IHRC 32MHz	High speed internal 32MHz RC. XIN/XOUT pins are bi-direction GPIO mode
	X'tal 12MHz	High speed crystal /resonator (e.g. 8MHz~24MHz) for external high clock oscillator
	X'tal 4MHz	Standard crystal /resonator (e.g. 1MHz~8MHz) for external high clock oscillator
	External Clock	XIN pin connect external clock (1MHz~32MHz), XOUT pin is bi-direction GPIO mode
CPU Clock Rate	000 = Fhosc / 1 001 = Fhosc / 2 010 = Fhosc / 4 011 = Fhosc / 8 100 = Fhosc / 16 101 = Fhosc / 32 110 = Fhosc / 64 111 = Fhosc / 128	Fcpu clock rate
CK_Fine_Tuning	Disable	Disable CK_Fine_Tuning
	Enable	Enable CK_Fine_Tuning
LVD De-bounce	Disable	LVD 1.7V reset without De-bounce.
	4* F_{ILRC}	LVD 1.7V reset with 4* F_{ILRC} De-bounce.
	8* F_{ILRC}	LVD 1.7V reset with 8* F_{ILRC} De-bounce.
	16* F_{ILRC}	LVD 1.7V reset with 16* F_{ILRC} De-bounce.
External Reset	Reset with De-bounce	Enable External reset pin with De-bounce
	Reset without De-bounce	Enable External reset pin without De-bounce
	GPIO	Enable GPIO
Watchdog Reset	Always	Watchdog timer is always on enable even in STOP mode and IDLE mode
	Enable	Enable watchdog timer. Watchdog timer stops in STOP mode and IDLE mode
	Disable	Disable Watchdog function
Watchdog Overflow Period	64ms	Watchdog timer clock source F_{ILRC} /4
	128ms	Watchdog timer clock source F_{ILRC} /8
	256ms	Watchdog timer clock source F_{ILRC} /16
	512ms	Watchdog timer clock source F_{ILRC} /32

Low Speed Clock Source	LXTAL	Low speed 32.768 KHz crystal
	ILRC	Low speed internal RC. LXIN/LXOUT pins are bi-direction GPIO mode

7.2 Power-on Sequence

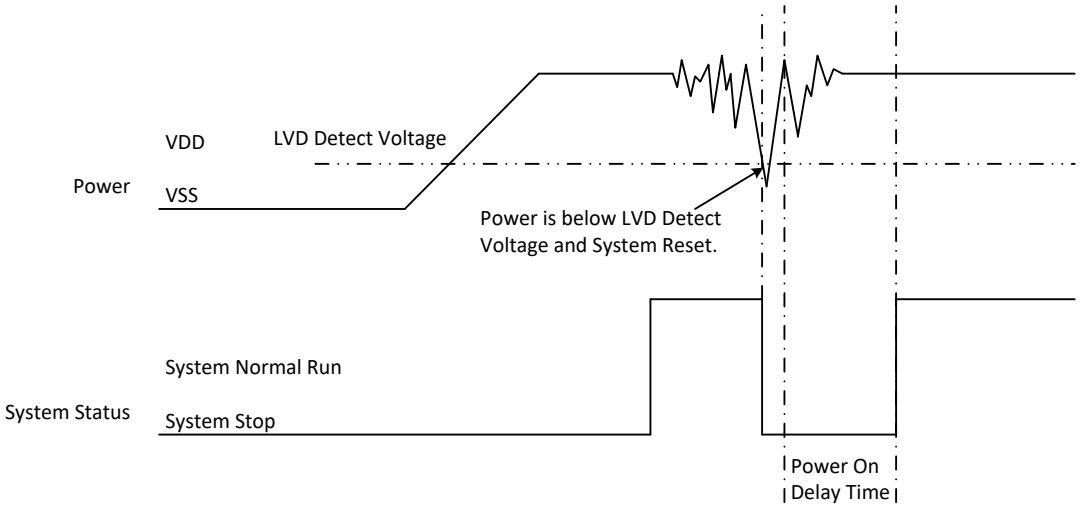
A power-on sequence would be triggered by LVD, watchdog, and external reset pin. It takes place between the end of reset signal and program execution. Overall, it includes two stages: power stabilization period, and clock stabilization period.



The power stabilization period spends 6.7 ms in typical condition. Afterward the microcontroller fetches CPU Clock Source selection automatically. The selected clock source would be driven, and the system counts 2048 times of the clock period and 5 times of the internal low-speed oscillator clocks to ensure its reliability. Then power-on sequence is finished and program executes from boot loader.

7.3 LVD Reset

The low voltage detectors monitor VDD pin's voltage at only one level: 1.7 V. Depend on low voltage detection configuration, the comparison result can be seen as a system reset signal. The table below lists low voltage detection, and the results of VDD pin's condition.



Condition	LVD
VDD ≤ 1.7V - 3.6V	Reset

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDCON	-	-	INTLVL2	INTLVL1	INTLVL0	RSTLVL2	RSTLVL1	RSTLVL0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN2	EU3RX	EU3TX	-	-	-	ET2	EADC	ELVD
IRCON2	-	-	-	-	-	TF2	ADCF	LVDF

LVDCON Register (0xE7)

Bit	Field	Type	Initial	Description
7..6	Reserved	R	0x0	
5..3	INTLVL[2:0]	R/W	000	LVD flag voltage by selection 000: 1.7V 001: 2.0V 010: 2.2V 011: 2.4V 100: 2.7V

				101: 3.0V 110: 3.3V 111: 3.6V
2..0	RSTLVL[2:0]	R/W	000	LVD reset voltage by selection 000: 1.7V 001: 2.0V 010: 2.2V 011: 2.4V 100: 2.7V 101: 3.0V 110: 3.3V 111: 3.6V

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN2 Register (0xC8)

Bit	Field	Type	Initial	Description
0	ELVD	R/W	0	LVD interrupt control bit. 0: Disable LVD interrupt function. 1: Enable LVD interrupt function.
Else				Refer to other chapter(s)

IRCON2 Register (0xA7)

Bit	Field	Type	Initial	Description
0	LVDF	R/W	0	LVD interrupt request flag. 0: None LVD interrupt request 1: LVD interrupt request.
Else				Refer to other chapter(s)

7.4 Watchdog Reset

Watchdog is a periodic reset signal generator for the purpose of monitoring the execution flow. Its internal timer is expected to be cleared in a check point of program flow; therefore, the actual reset signal would be generated only after a software problem occurs. Writing 0x5A to WDTR is the proper method to place a check point in program.

```
1     WDTR = 0x5A;
```

Watchdog timer interval time = 256 * 1/ (Internal Low-Speed oscillator frequency/WDT Pre-scalar)
= 256 / (F_{ILRC} /WDT Pre-scaler) …sec

Internal low-speed oscillator	WDT pre-scaler	Watchdog interval time
F_{ILRC} =16 kHz	F_{ILRC} /4	256/(16000/4)=64ms
	F_{ILRC} /8	256/(16000/8)=128ms
	F_{ILRC} /16	256/(16000/16)=256ms
	F_{ILRC} /32	256/(16000/32)=512ms

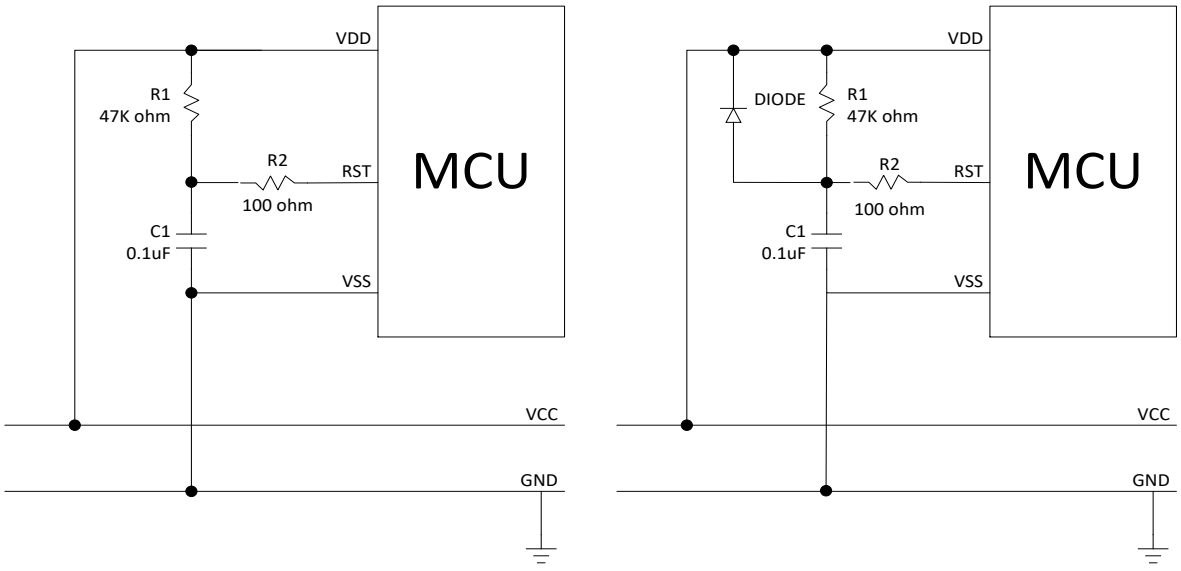
The operation mode of watchdog is configurable in options file:
Always mode counts its internal timer in all CPU operation modes (normal, IDLE, SLEEP);
Enable mode counts its internal timer during CPU stays in normal mode, and it would not trigger watchdog reset in IDLE and STOP modes;
Disable mode suspends its internal timer at all CPU modes, and the watchdog would not trigger in this condition.

When watchdog is operating in always mode, the system will consume additional power.

7.5 External Reset Pin

Programmable external reset pin is configurable in *options file*. Once it is enabled, it monitors its shared pin's logic level. A logical low (lower than 30% of VDD) would immediately trigger system reset until the input is recovered to high (lager than 70% of VDD).

An optional de-bounce period can improve reset signal's stability. Instead of immediate reset, the system reset requires an 8-ms-long logic low to avoid bouncing from a button key. Any signal lower than de-bounce period would not affect the CPU's execution.



✸ ***Note:***

1. The reset circuit is no any protection against unusual power or brown out reset on the left side of the figure.

2. The R2 100 ohm resistor of "Simply reset circuit" and "Diode & RC reset circuit" is necessary to limit any current flowing into reset pin from external capacitor C in the event of reset pin breakdown due to Electrostatic Discharge (ESD) or Electrical Over-stress (EOS) on the right side of the figure.

7.6 Software Reset

A software reset would be generated after consecutively set SRSTREQ register. As a result, this procedure enables firmware's ability to reset microcontroller (e.g. reset after firmware update). The following sample C code repeatedly set the least bit of SRST register to perform software reset.

```
1   SRST = 0x01;
2   SRST = 0x01;
```

7.7 Reset and Power-on Controller Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PFLAG	POR	WDT	RST	WARM	-	-	-	-
SRST	-	-	-	-	-	-	-	SRSTREQ
WDTR	WDTR7	WDTR6	WDTR5	WDTR4	WDTR3	WDTR2	WDTR1	WDTR0

PFLAG Register (0xFF)

Bit	Field	Type	Initial	Description
7	POR	R	-	This bit is automatically set if the microcontroller has been reset by LVD.
6	WDT	R	-	This bit is automatically set if the microcontroller has been reset by watchdog.
5	RST	R	-	This bit is automatically set if the microcontroller has been reset by external reset pin.
4	WARM	R	0	This bit is automatically set if the Ext. 32.768kHz crystal warm up is ready.
3..0	Reserved	R	0	

SRST Register (0xF7)

Bit	Field	Type	Initial	Description
7..1	Reserved	R	0	
0	SRSTREQ	R/W	-	Read: This bit is automatically set if the microcontroller has been reset by software reset. Write: Consecutively set this bit for two times to trigger software reset.

WDTR Register (0x86)

Bit	Field	Type	Initial	Description
7..0	WDTR[7:0]	W	-	Watchdog clear is controlled by WDTR register. Moving 0x5A data into WDTR is to reset watchdog timer.

8 System Clock and Power Management

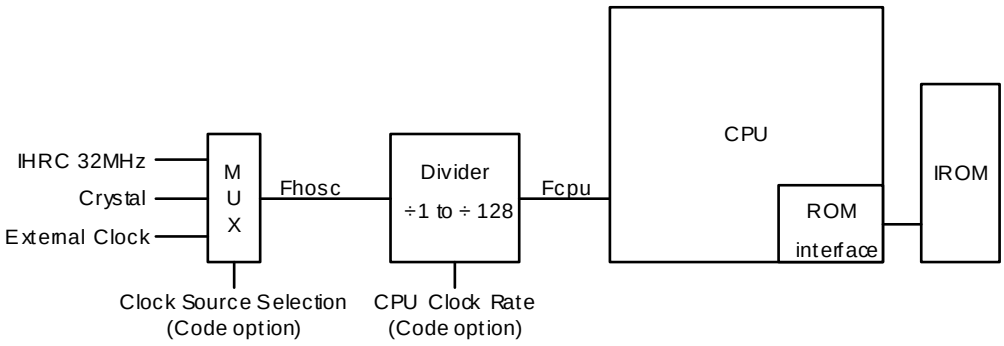
For power saving purpose, the microcontroller built in three different operation modes: normal, IDLE, and STOP mode.

The normal mode means that CPU and peripheral functions are under normally execution. The system clock is based on the combination of source selection, clock divider, and program memory wait state. IDLE mode is the situation that temporarily suspends CPU clock and its execution, yet it remains peripherals' functionality (e.g. timers, PWM, UART, and I2C). STOP mode disables all functions and clock generator until a wakeup signal to return normal mode.

8.1 System Clock

The microcontroller includes an on-chip clock generator (IHRC 32MHz), crystal/resonator driver, and an external clock input. The reset and power-on controller automatically loads clock source selection during power-on sequence. Therefore, the selected clock source is seen as 'Fhosc' domain which is a fixed frequency at any time.

Subsequently, the selected clock source (Fhosc) is divided by 1 to 128 times which is controlled by code option.



ROM interface is built in between CPU and IROM (program memory). It optionally extends the data fetching cycle in order to support lower speed program memory.

IROM fetching cycle (Instruction cycle) ≦ 24MHz

✷ ***Note: CPU clock source from IHRC limit divider = 2, CPU clock source from others don't limit divider.***

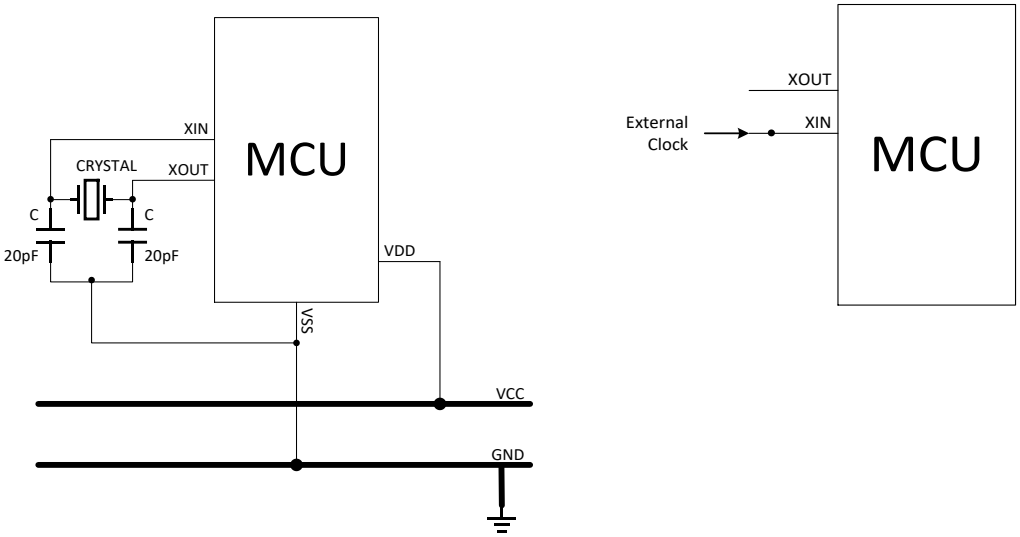
System clock rate and program memory extended cycle limitation as follows.

	CPU Clock Source		
CPU Clock Rate	IHRC 32M	X'tal 12M / X'tal 4M	External Clock (1-32MHz)
000 = Fhosc / 1	-	V	V (Clock < 24MHz)
001 = Fhosc / 2	V	V	V
010 = Fhosc / 4	V	V	V
011 = Fhosc / 8	V	V	V
100 = Fhosc / 16	V	V	V
101 = Fhosc / 32	V	V	V
110 = Fhosc / 64	V	V	V
110 = Fhosc / 128	V	V	V

8.2 High Speed Clock

High-speed clock has internal and external two-type. The external high-speed clock includes 4MHz, 12MHz crystal/ceramic and external clock input mode. The internal high-speed oscillator is 32MHz RC type. These high-speed oscillators are selected by *SN8F5869_OPTIONS.A51*.

Mode	Clock Source Type	Frequency	XIN/XOUT Pin	External Components	Capacitor to GND
IHRC 32M	Internal RC oscillator	32 MHz	XIN/XOUT = GPIO	None	N/A
X'tal 12M	External crystal/ ceramic oscillator	8 MHz ~ 24 MHz	XIN/XOUT = Connected to crystal/ceramic	Crystal or ceramic resonator	20 pF
X'tal 4M		1MHz ~ 8MHz			20 pF
External Clock	External clock input	Depends on external source	XIN = External clock input XOUT = GPIO	External clock source (XIN only)	N/A

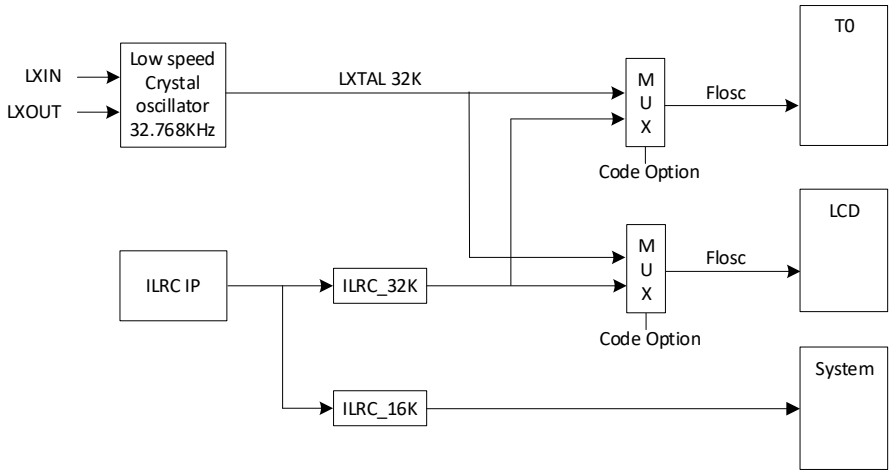


8.3 Low Speed Clock

Low-speed clock has internal and external two-type. The external low-speed clock is 32.768 kHz crystal (LXTAL_32K). The internal low-speed oscillator is RC type which can support two kinds of frequency, ILRC_16K and ILRC_32K. ILRC_16K is only used for system operation. Only LXTAL_32K and ILRC_32K can be selected as low speed clock (Flosc) for specific functions, such as T0 and LCD. These low-speed oscillators are selected by *SN8F5869_OPTIONS.A51*.

Mode	Clock Source Type	Frequency	XIN/XOUT Pin	External Components	Capacitor to GND
ILRC 32K	Internal RC oscillator	32 KHz	XIN/XOUT = GPIO	None	N/A
LXTAL	RTC crystal	32.768 kHz (RTC)	XIN/XOUT = Crystal mode for 32.768 kHz crystal	32.768 kHz crystal	20 pF

Microcontroller supplies WARM bit (the 4th bit of PFLAG) to indicate crystal warm-up status. The WARM bit is set when crystal warm-up procedure ready and cleared when crystal stop.



8.4 Noise Filter

The Noise Filter controlled by Noise Filter option is a low pass filter and supports crystal mode. The purpose is to filter high rate noise coupling on high clock signal from external oscillator. In high noisy environment, enable Noise Filter option is the strongly recommendation to reduce noise effect.

8.5 Power Management

After the end of reset signal and power-on sequence, the CPU starts program execution at the speed of Fcpu. Overall, the CPU and all peripherals are functional in this situation (categorized as normal mode).

The least two bits of PCON register (IDLE at bit 0 and STOP at bit 1) control the microcontroller's power management unit.

If IDLE bit is set by program, only CPU clock source would be gated. Consequently, peripheral functions (such as timers, PWM, and I2C) and clock generator (IHRC 32 MHz/crystal driver) remain execution in this status. Any change from P0/P1 input and interrupt events can make the microcontroller turns back to normal mode, and the IDLE bit would be cleared automatically.

If STOP bit is set, by contrast, CPU, peripheral functions, and clock generator are suspended. Data storage in registers and RAM would be kept in this mode. Any change from P0/P1 can wake up the microcontroller and resume system's execution. STOP bit would be cleared automatically.

For user who is develop program in C language, IDLE and STOP macros is strongly recommended to control the microcontroller's system mode, instead of set IDLE and STOP bits directly.

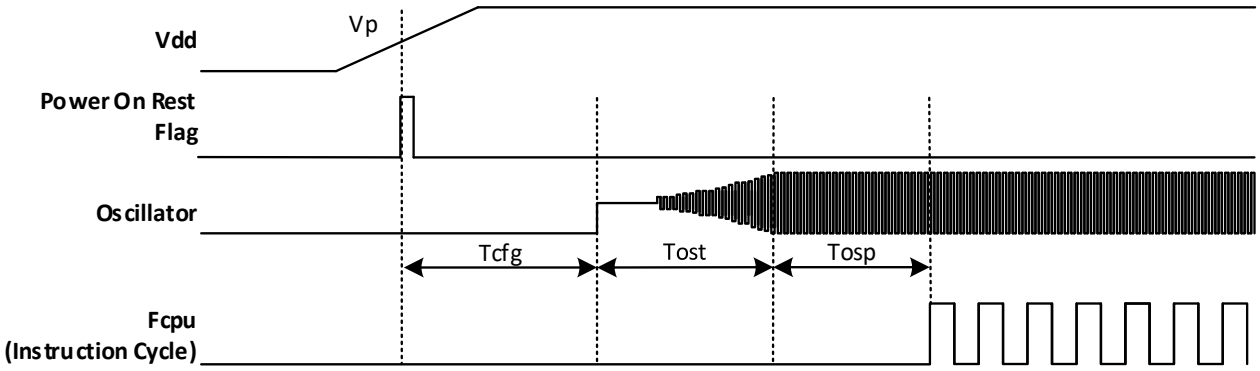
```
1     IDLE();
2     STOP();
```

SN8F5869 build in STWK bit (the 0th bit in SYSMOD register) to enable or disable Flosc clock in STOP mode. If STWK=0, both Fhosc and Flosc are suspended in STOP mode. If STWK=1, Flosc clock keeps running in STOP mode.

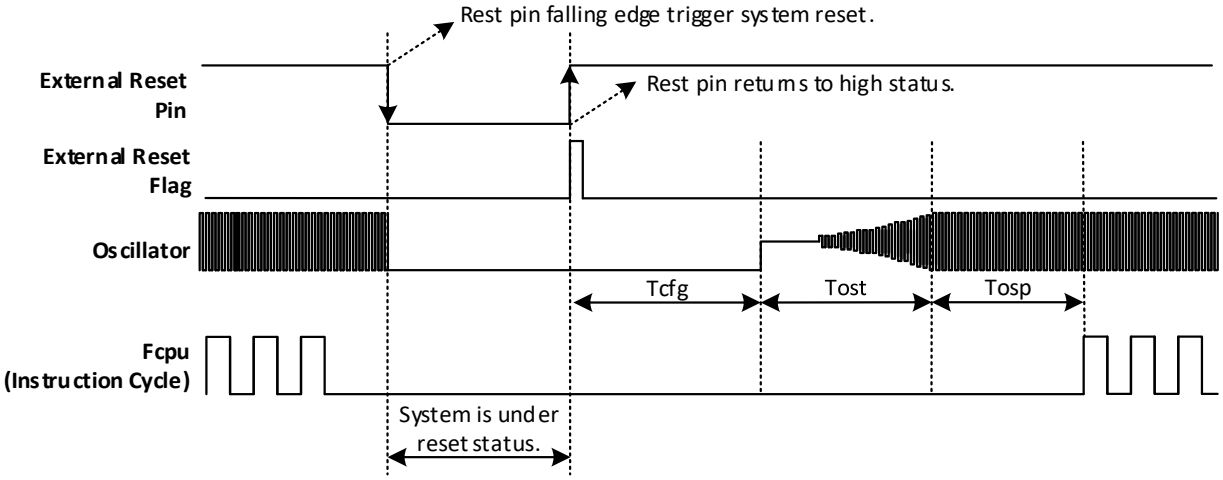
8.6 System Clock Timing

Parameter	Symbol	Description	Typical
Hardware configuration time	Tcfg	11* F_{ILRC} + 2^{17}*F_{IHRC}	4.78ms @ F_{ILRC} = 16kHz & F_{IHRC} = 32MHz
Oscillator start up time	Tost	The start-up time is depended on oscillator's material, factory and architecture. Normally, the low-speed oscillator's start-up time is lower than high-speed oscillator. The RC type oscillator's start-up time is faster than crystal type oscillator.	
Oscillator warm-up time	Tosp	Oscillator warm-up time of reset condition. 2ms + 2^{13}*F_{hosc}……Crystal/resonator type oscillator, e.g. 4MHz crystal, 16MHz crystal… 2ms……RC type oscillator, e.g. internal high-speed RC type oscillator. (Power on reset, LVD reset, watchdog reset, external reset pin active.)	X'tal: 4.05ms @ F_{hosc} = 4MHz 2.51us @ F_{hosc} = 16MHz RC: 2ms @ F_{hosc} = 32MHz
		Oscillator warm-up time of power down mode wake-up condition. 2.5*F_{ILRC} + 2^{13}*F_{hosc} ……Crystal/resonator type oscillator, e.g. 4MHz crystal, 16MHz crystal… 4*F_{ILRC}……RC type oscillator, e.g. internal high-speed RC type oscillator.	X'tal: 2.2ms @ F_{hosc} = 4MHz 668us @ F_{hosc} = 16MHz RC: 250us @ F_{hosc} = 32MHz
		Oscillator warm-up time of idle down mode wake-up condition. 3*F_{ILRC}……RC type oscillator, e.g. internal high-speed RC type oscillator.	188us @ F_{ILRC} = 16kHz & F_{IHRC} = 32MHz

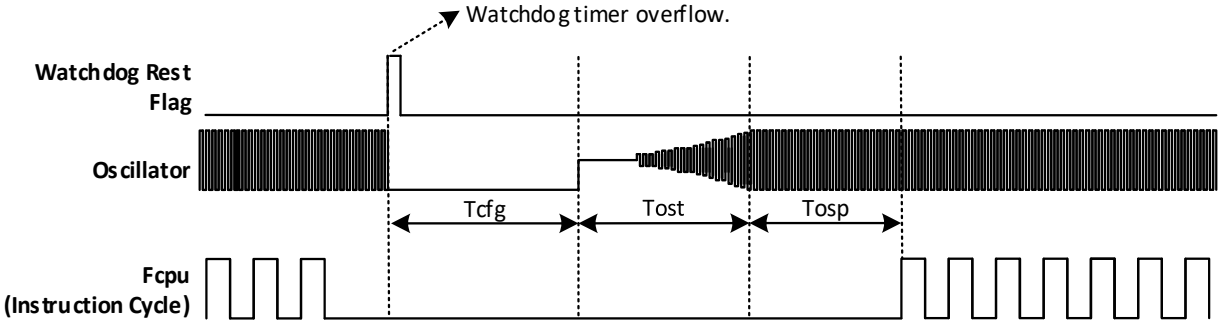
- Power On Reset Timing



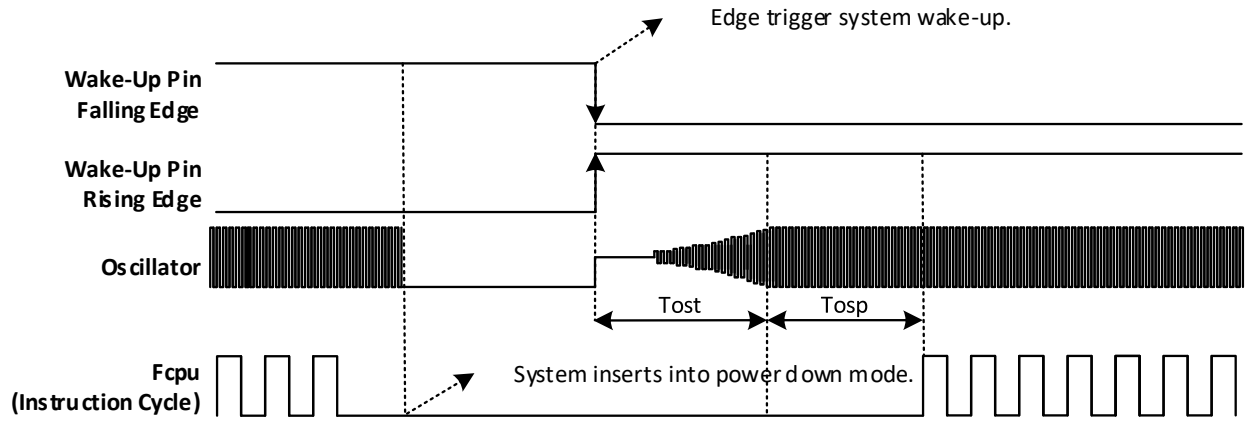
- External Reset Pin Reset Timing



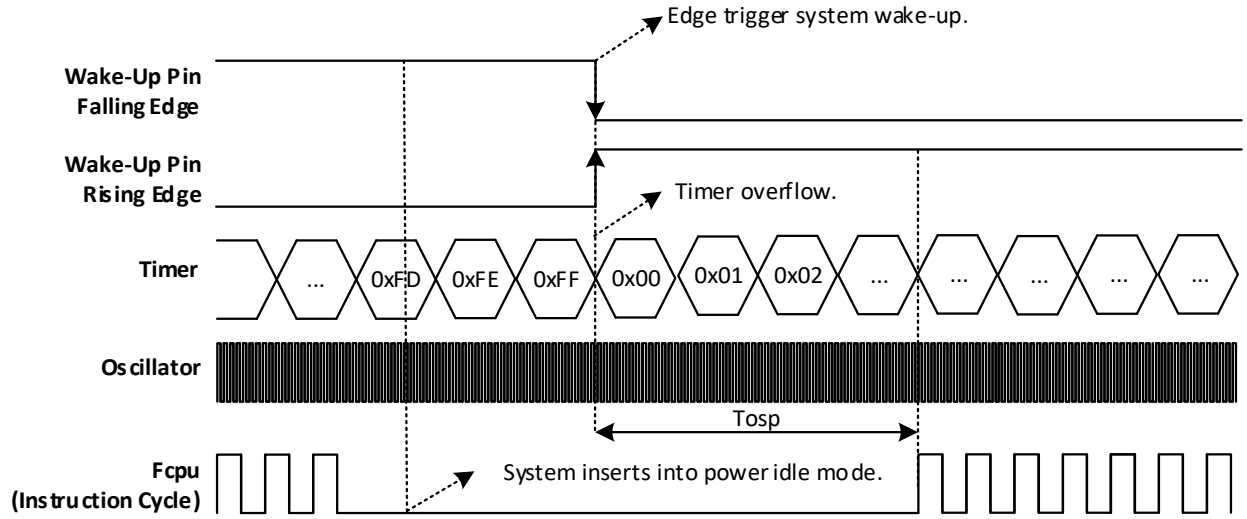
- Watchdog Reset Timing



- STOP Mode Wake-up Timing

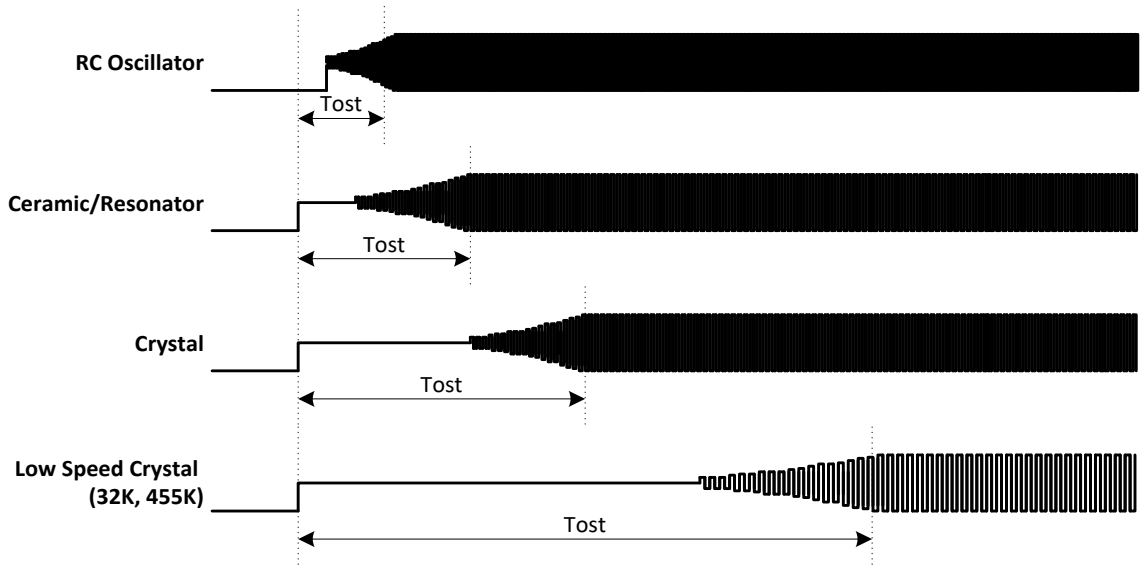


- IDLE Mode Wake-up Timing



- Oscillator Start-up Time

The start-up time is depended on oscillator's material, factory and architecture. Normally, the low-speed oscillator's start-up time is lower than high-speed oscillator.



8.7 System Clock and Power Management Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	-	-	-	-	-	GF0	STOP	IDLE
P1W	P17W	P16W	P15W	P14W	P13W	P12W	P11W	P10W
SYSMOD	-	-	-	-	-	-	-	STWK

PCON Register (0x87)

Bit	Field	Type	Initial	Description
7..3	Reserved	R	0	
2	GF0	R/W	0	General Purpose Flag
1	STOP	R/W	0	1: Microcontroller switch to STOP mode
0	IDLE	R/W	0	1: Microcontroller switch to IDLE mode

P1W Register (0xC3)

Bit	Field	Type	Initial	Description
7..0	P1nW	R/W	0	0: Disable P1.n wakeup functionality 1: Enable P1.n wakeup functionality

SYSMOD Register (0xF4)

Bit	Field	Type	Initial	Description
7..1	Reserved	R	0x00	
0	STWK	R/W	0	0: Both Fhosc and Flosc are suspended in STOP mode. 1: Flosc keep running in STOP mode*.

* Before entering STOP mode, the STWK bit setting must be earlier than the STOP bit.

9 System Operating Mode

The chip builds in three operating mode for difference clock rate and power saving reason. These modes control oscillators, op-code operation and analog peripheral devices' operation.

- Normal mode: System high-speed operating mode
- IDLE mode: System idle mode (Green mode)
- STOP mode: System power saving mode (Sleep mode)

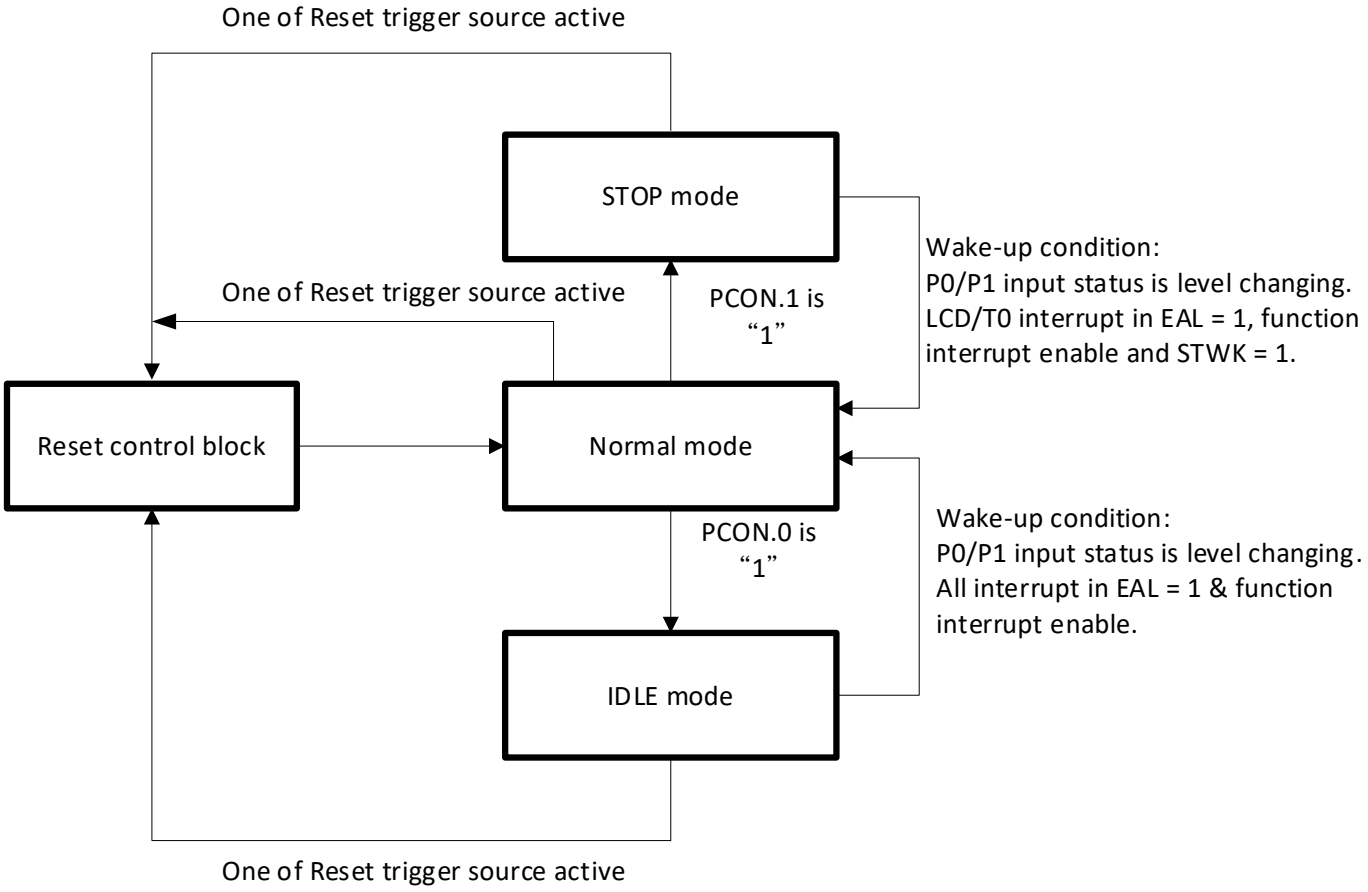


Table 9-1 The operating mode clock control

Operating Mode	Normal Mode	IDLE Mode	STOP Mode
IHRC	IHRC: Running Ext. OSC: Disable	IHRC: Running Ext. OSC: Disable	Stop
ILRC	Running	Running	STWK=1 & Code Option= ILRC: Running Watchdog always: Running
Ext. OSC	IHRC: Disable Ext. OSC : Running	IHRC: Disable Ext. OSC : Running	Stop

Ext. low OSC	Active as Code Option = Ext. 32kHz	Active as Code Option = Ext. 32kHz	Active as STWK=1 & Code Option = Ext. 32kHz
CPU instruction	Executing	Stop	Stop
Timer 0 (Timer, Event counter)	Active by TR0	Active by TR0	Active as Timer 0 clock source is Flosc (ILRC or Ext. 32kHz) & STWK=1
Timer 1 (Timer, Event counter)	Active by TR1	Active by TR1	Inactive
Timer 2 (Timer, capture)	Active as enable	Active as enable	Inactive
Timer 3/4	Active as enable	Active as enable	Inactive
PWM1/2/3/4	Active as enable	Active as enable	Inactive
UART0/1/2	Active as enable	Active as enable	Inactive
I2C	Active as enable	Active as enable	Inactive
LCD	Active as enable	Active as enable	Active as STWK = 1
ADC	Active as enable	Active as enable	Inactive
Watchdog timer	By Watchdog Code option	By Watchdog Code option	By Watchdog Code option
Internal interrupt	All active	All active	T0 interrupt is active when STWK = 1 and clock source is Flosc. Other inactive.
External interrupt	All active	All active	All inactive
Wakeup source	-	P0, P1, Reset, All interrupt in EAL = 1 & function interrupt enable	P0, P1, Reset, T0 enable & clock source is Flosc (ILRC or Ext. 32kHz) & STWK=1 & function interrupt enable.

- Ext. OSC: External high-speed oscillator (XIN/XOUT).
- Ext. low OSC: External low-speed oscillator (LXIN/LXOUT).
- IHRC: Internal high-speed oscillator RC type.
- ILRC: Internal low-speed oscillator RC type.

9.1 Normal Mode

The Normal Mode is system high clock operating mode. The system clock source is from high speed oscillator. The program is executed. After power on and any reset trigger released, the system inserts into normal mode to execute program. When the system is wake-up from STOP/IDLE mode, the system also inserts into normal mode. In normal mode, the high speed oscillator is active, and the power consumption is largest of all operating modes.

- The program is executed, and full functions are controllable.
- The system rate is high speed.
- The high speed oscillator and internal low speed RC type oscillator are active.
- Normal mode can be switched to other operating modes through PCON register.
- STOP/IDLE mode is wake-up to normal mode.

9.2 STOP Mode

The STOP mode is the system ideal status. No program execution and oscillator operation. Only internal regulator is active to keep all control gates status, register status and SRAM contents. The STOP mode is waked up by P0/P1 hardware level change trigger. P0 wake-up function is always enables. The STOP mode is wake-up to normal mode. Inserting STOP mode is controlled by stop bit of PCON register. When stop = 1, the system inserts into STOP Mode. After system wake-up from STOP mode, the stop bit is disabled (zero status) automatically.

- The program stops executing, and full functions are disabled.
- All oscillators including external high speed oscillator, internal high speed oscillator and internal low speed oscillator stop.
- Only internal regulator is active to keep all control gates status, register status and SRAM contents.
- The system inserts into normal mode after wake-up from STOP mode.
- The STOP mode wake-up source is P0/P1 level change trigger, T0 enable & clock source is Flosc (ILRC or Ext. 32kHz) & STWK=1 & function interrupt enable.

9.3 IDLE Mode

The IDLE mode is another system ideal status not like STOP mode. In STOP mode, all functions and hardware devices are disabled. But in IDLE mode, the system clock source keeps running, so the power consumption of IDLE mode is larger than STOP mode. In IDLE mode, the program isn't executed, but the timer with wake-up function is active as enabled, and the timer clock source is the non-stop system clock. The IDLE mode has 2 wake-up sources. One is the P0/P1 level change trigger wake-up. The other one is any interrupt in EAL = 1 & function interrupt enable. That's mean users can setup any function with interrupt enable, and the system is waked up until the interrupt issue. Inserting IDLE mode is controlled by idle bit of PCON register. When idle = 1, the system inserts into IDLE mode. After system wake-up from IDLE mode, the idle bit is disabled (zero status) automatically.

- The program stops executing, and full functions are disabled.
- The oscillator to be the system clock source keeps running, and the other oscillators operation is depend on system operation mode configuration.
- If inserting IDLE mode from normal mode, the system insets to normal mode after wake-up.
- The IDLE mode wake-up sources are P0/P1 level change trigger.
- If the function clock source is system clock, the functions are workable as enabled and under IDLE mode, e.g. Timer, PWM, event counter…
- All interrupt in EAL = 1 & function interrupt enable can wake-up in IDLE mode.

9.4 Wake up

Under STOP mode (sleep mode) or idle mode, program doesn't execute. The wakeup trigger can wake the system up to normal mode. The wakeup trigger sources are external trigger (P0/P1 level change) and internal trigger (any interrupt in EAL = 1 & function interrupt enable). The wakeup function builds in interrupt operation issued request flag and trigger system executing interrupt service routine as system wakeup occurrence.

Parameter	Symbol	Description	Typical
Oscillator warm-up time	Tosp	Oscillator warm-up time of power down mode wake-up condition. $2.5*F_{ILRC} + 2^{13}*F_{hosc}$ ……Crystal/resonator type oscillator, e.g. 4MHz crystal, 16MHz crystal… $4*F_{ILRC}$……RC type oscillator, e.g. internal high-speed RC type oscillator.	X'tal: 2.2ms @ F_{hosc} = 4MHz 668us @ F_{hosc} = 16MHz RC: 250us @ F_{hosc} = 32MHz
		Oscillator warm-up time of idle down mode wake-up condition. $3*F_{ILRC}$……RC type oscillator, e.g. internal high-speed RC type oscillator.	188us @ F_{ILRC} = 16kHz & F_{IHRC} = 32MHz

When the system is in STOP mode the high clock oscillator stops. When waked up from STOP mode, MCU waits for 8192 external high-speed oscillator clocks + 2.5 internal low-speed oscillator clocks and 4 internal low-speed oscillator clocks as the wakeup time to stable the oscillator circuit. When waked up from IDLE mode, MCU waits for 3 internal low-speed oscillator clocks. After the wakeup time, the system goes into the normal mode.

The value of the external high clock oscillator wakeup time is as the following.

The Wakeup time = $1/F_{ILRC}$ *2.5 + $1/F_{hosc}$ * 8192 + high clock start-up time (STOP mode)

The Wakeup time = 1/Flosc * 5 (IDLE mode)

Example: In STOP mode (sleep mode), the system is waked up. After the wakeup time, the system goes into normal mode. The wakeup time is as the following.

The wakeup time = $1/F_{ILRC}$ *2.5 + $1/F_{hosc}$ * 8192 = 668 us (F_{hosc}= 16MHz)

The total wakeup time = 668 us + oscillator start-up time

The value of the internal high clock oscillator RC type wakeup time is as the following.

The Wakeup time = $1/F_{ILRC}$ *4 + high clock start-up time

Example: In STOP mode (sleep mode), the system is waked up. After the wakeup time, the system

goes into normal mode. The wakeup time is as the following.

The wakeup time = $1/F_{ILRC}$ *4 = 250 us+ high clock start-up time (F_{hosc} = 32MHz)

✷ ***Note: The high clock start-up time is depended on the VDD and oscillator type of high clock.***

Under STOP mode and green mode, the I/O ports with wakeup function are able to wake the system up to normal mode. The wake-up trigger edge is level changing in rising edge or falling edge. The Port 0 and Port 1 have wakeup function. Port 0 wakeup functions always enables, but the Port 1 is controlled by the P1W register.

P1W Register (0xC3)

Bit	Field	Type	Initial	Description
7..0	P1nW	R/W	0	0: Disable P1.n wakeup functionality 1: Enable P1.n wakeup functionality

10 Interrupt

The MCU provides 23 interrupt sources (5 external and 18 interrupt) with 4 priority levels. Each interrupt source includes one or more interrupt request flag(s). When interrupt event occurs, the associated interrupt flag is set to logic 1. If both interrupt enable bit and global interrupt (EAL=1) are enabled, the interrupt request is generated and interrupt service routine (ISR) will be started. Some interrupt request flags must be cleared by software. However, most interrupt request flags can be cleared by hardware automatically. In the end, ISR is finished after complete the RETI instruction. The summary of interrupt source, interrupt vector, priority order and control bit are shown as the table below.

Table 10-1 The interrupt list

Interrupt	Enable Interrupt	Request (IRQ)	IRQ Clearance	Priority / Vector
System Reset	-	-	-	0 / 0x0000
TIMER0	ET0	TF0	Automatically	2 / 0x000B
INT1	EX1	IE1	Automatically	3 / 0x0013
TIMER1	EX1	TF1	Automatically	4 / 0x001B
INT2	EX2	IE2	Automatically	5 / 0x0023
TIMER2	ET2	TF2	Automatically	6 / 0x002B
TIMER3	ET3	TF3	Automatically	7 / 0x0033
INT3	EX3	IE3	Automatically	8 / 0x003B
I2C	EI2C	SI	By firmware	9 / 0x0043
SPI	ESPI	SPIF & MODF	By firmware	10 / 0x004B
UART0 RX	EU0RX	RI0	By firmware	11 / 0x0053
UART0 TX	EU0TX	TI0	By firmware	12 / 0x005B
UART1 RX	EU1RX	RI1	By firmware	13 / 0x0063
UART1 TX	EU1TX	TI1	By firmware	14 / 0x006B
TIMER4	ET4	TF4	Automatically	15 / 0x0073
INT4	EX4	IE4	Automatically	16 / 0x007B
PWM1	EPW1	PW1F	Automatically	17 / 0x0083
PWM2	EPW2	PW2F	Automatically	18 / 0x008B
PWM3	EPW3	PW3F	Automatically	19 / 0x0093
ADC	EADC	ADCF	Automatically	20 / 0x00AB
LVD	ELVD	LVDF	Automatically	21 / 0x00BB
UART3 TX	EU3TX	TI3	By firmware	22 / 0x00C3
UART3 RX	EU3RX	RI3	By firmware	23 / 0x00CB
UART2 TX	EU2TX	TI2	By firmware	24 / 0x00D3
UART2 RX	EU2RX	RI2	By firmware	25 / 0x00DB
PWM4	EPW4	PW4F	Automatically	26 / 0x00E3

10.1 Interrupt Operation

Interrupt operation is controlled by interrupt request flag and interrupt enable bits. Interrupt request flag is interrupt source event indicator, no matter what interrupt function status (enable or disable). Both interrupt enable bit and global interrupt (EAL=1) are enabled, the system executes interrupt operation when each of interrupt request flags is active. The program counter points to interrupt vector (0x03 – 0xEB) and execute ISR.

10.2 Interrupt Priority

Each interrupt source has its specific default priority order. If two interrupts occurs simultaneously, the higher priority ISR will be service first. The lower priority ISR will be serviced after the higher priority ISR completes. The next ISR will be service after the previous ISR complete, no matter the priority order.

For special priority needs, 4-level priority levels (Level 0 – Level 3) are used. All interrupt sources are classified into 6 priority groups (Group0 – Group5). Each group can be set one specific priority level. Priority level is selected by IP0/IP1 registers. Level 3 is the highest priority and Level 0 is the lowest. The interrupt sources inside the same group will share the same priority level. With the same priority level, the priority rule follows default priority.

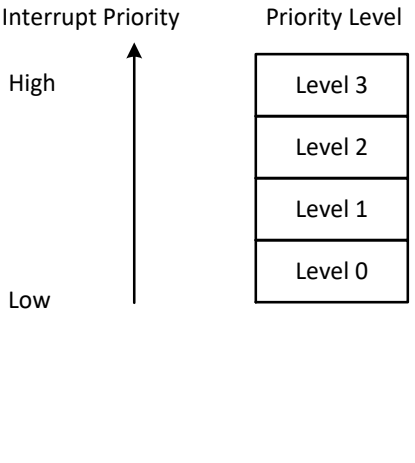
Priority Level	IP1.x	IP0.x
Level 0	0	0
Level 1	0	1
Level 2	1	0
Level 3	1	1

The ISR with the higher priority level can be serviced first; even can break the on-going ISR with the lower priority level. The ISR with the lower priority level will be pending until the ISR with the higher priority level completes.

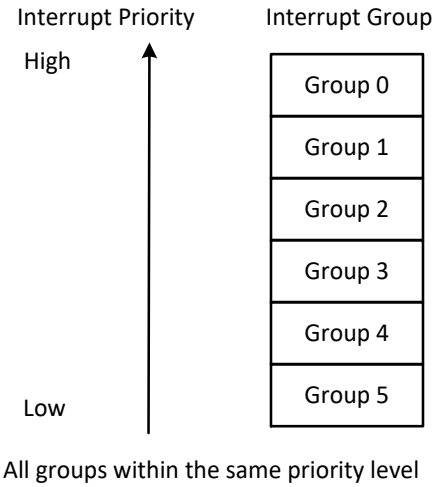
Group	Interrupt Source				
Group 0	-	TIMER3	PWM1	UART3 TX	I2C
Group 1	TIMER0	INT3	PWM2	UART3 RX	SPI
Group 2	INT1	TIMER4	PWM3	UART2 TX	UART0 RX
Group 3	TIMER1	INT4	-	UART2 RX	UART0 TX
Group 4	INT2	-	-	PWM4	UART1 RX
Group 5	TIMER2	LVD	ADC	-	UART1 TX

When more than one interrupt request occur, the highest priority request must be executed first. Choose the highest priority request according natural priority and priority level. The steps are as the following:

1. Choose the groups which have the highest priority level between all groups.
2. Choose the group which is the highest nature priority between the groups with the highest priority level.
3. Choose the ISR which has the highest nature priority inside the group with the highest priority.



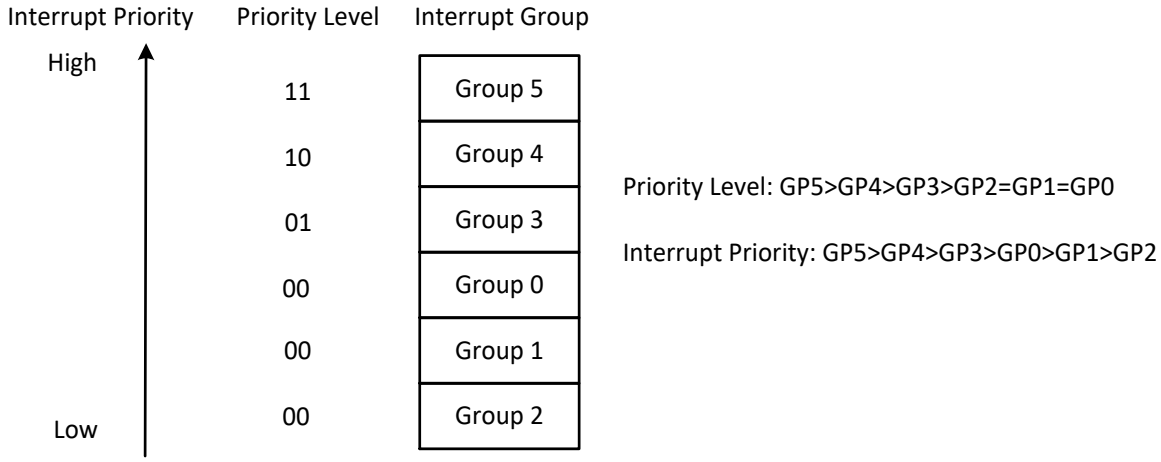
Higher priority level has higher priority



All groups within the same priority level
IP0.0 = IP0.1 = IP0.2 = IP0.3 = IP0.4 = IP0.5
IP1.0 = IP1.1 = IP1.2 = IP1.3 = IP1.4 = IP1.5

As the example, group5 has the highest priority level and group0~group2 have the lowest priority level. It means the interrupt vector in group5 has the highest interrupt priority, the 2nd interrupt priority in group4 and the 3rd interrupt priority in group3. Group0~ group2 have the same priority level thus the nature priority rule will be followed. Therefore, interrupt priority will be group5> group4> group3> group0> group1> group2.

```
MOV     IP0, #00101000B         ; Set group0 - group5 in different priority level.
MOV     IP1, #00110000B
```



IP0, IP1 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP0	-	-	IP05	IP04	IP03	IP02	IP01	IP00
IP1	-	-	IP15	IP14	IP13	IP12	IP11	IP10

IP0 Register (0xA9)

Bit	Field	Type	Initial	Description
5..0	IP0[5:0]	R/W	0	Interrupt priority. Each bit together with corresponding bit from IP1 register specifies the priority level of the respective interrupt priority group.
Else	Reserved	R	0	

IP1 Register (0xB9)

Bit	Field	Type	Initial	Description
5..0	IP1[5:0]	R/W	0	Interrupt priority. Each bit together with corresponding bit from IP0 register specifies the priority level of the respective interrupt priority group.
Else	Reserved	R	0	

10.3 Interrupt Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	-
IEN1	EU2RX	EU2TX	EU1RX	EU1TX	EU0RX	EU0TX	ESPI	EI2C

IEN2	EU3RX	EU3TX	-	-	-	ET2	EADC	ELVD
IEN3	ET4	ET3	EPW4	EPW3	EPW2	EPW1	-	-
IRCON0	-	IE4	IE3	IE2	-	-	-	-
IRCON2	-	-	-	-	-	TF2	ADCF	LVDF
IRCON3	TF4	TF3	PW4F	PW3F	PW2F	PW1F	-	-
TCON	TF1	TR1	TF0	TR0	IE1	-	-	-
S0CON	S0M0	S0M1	S0M20	REN0	TB80	RB80	TI0	RI0
S1CON	S1M0	S1M1	S1M20	REN1	TB81	RB81	TI1	RI1
S2CON	S2M0	S2M1	S2M20	REN2	TB82	RB82	TI2	RI2
I2CCON	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
SPSTA	SPIF	WCOL	SSERR	MODF	-	-	-	SPIMX

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Enable all interrupt control bit. 0: Disable all interrupt function. 1: Enable all interrupt function.
6	EX4	R/W	0	External P2.4 interrupt (INT4) control bit. 0: Disable INT4 interrupt function. 1: Enable INT4 interrupt function.
5	EX3	R/W	0	External P2.3 interrupt (INT3) control bit. 0: Disable INT3 interrupt function. 1: Enable INT3 interrupt function.
4	EX2	R/W	0	External P2.2 interrupt (INT2) control bit. 0: Disable INT2 interrupt function. 1: Enable INT2 interrupt function.
3	ET1	R/W	0	T1 timer interrupt control bit. 0: Disable T1 interrupt function. 1: Enable T1 interrupt function.
2	EX1	R/W	0	External P2.1 interrupt (INT1) control bit. 0: Disable INT1 interrupt function. 1: Enable INT1 interrupt function.
1	ET0	R/W	0	T0 timer interrupt control bit. 0: Disable T0 interrupt function. 1: Enable T0 interrupt function
0	ReservedEX0	R/W	0	

IEN1 Register (0xB8)

Bit	Field	Type	Initial	Description
7	EU2RX	R/W	0	UART2 RX interrupt control bit. 0: Disable UART RX interrupt function. 1: Enable UART RX interrupt function.
6	EU2TX	R/W	0	UART2 TX interrupt control bit. 0: Disable UART TX interrupt function. 1: Enable UART TX interrupt function.
5	EU1RX	R/W	0	UART1 RX interrupt control bit. 0: Disable UART RX interrupt function. 1: Enable UART RX interrupt function.
4	EU1TX	R/W	0	UART1 TX interrupt control bit. 0: Disable UART TX interrupt function. 1: Enable UART TX interrupt function.
3	EU0RX	R/W	0	UART0 RX interrupt control bit. 0: Disable UART RX interrupt function. 1: Enable UART RX interrupt function.
2	EU0TX	R/W	0	UART0 TX interrupt control bit. 0: Disable UART TX interrupt function. 1: Enable UART TX interrupt function.
1	ESPI	R/W	0	SPI interrupt control bit. 0: Disable SPI interrupt function. 1: Enable SPI interrupt function.
0	EI2C	R/W	0	I2C interrupt control bit. 0: Disable I2C interrupt function. 1: Enable I2C interrupt function.

IEN2 Register (0xC8)

Bit	Field	Type	Initial	Description
7	EU3RX	R/W	0	UART3 RX interrupt control bit. 0: Disable UART RX interrupt function. 1: Enable UART RX interrupt function.
6	EU3TX	R/W	0	UART3 TX interrupt control bit. 0: Disable UART TX interrupt function. 1: Enable UART TX interrupt function.
5..3	Reserved	R	0	
2	ET2	R/W	0	Timer 2 interrupt control bit. 0: Disable T2 interrupt function.

				1: Enable T2 interrupt function.
1	EADC	R/W	0	ADC interrupt control bit. 0: Disable ADC interrupt function. 1: Enable ADC interrupt function.
0	ELVD	R/W	0	LVD interrupt control bit. 0 = Disable LVD interrupt function. 1 = Enable LVD interrupt function.

IEN3 Register (0xEC)

Bit	Field	Type	Initial	Description
7	ET4	R/W	0	Timer 4 interrupt control bit. 0: Disable T4 interrupt function. 1: Enable T4 interrupt function.
6	ET3	R/W	0	Timer 3 interrupt control bit. 0: Disable T3 interrupt function. 1: Enable T3 interrupt function.
5	EPW4	R/W	0	PWM4 interrupt control bit. 0 = Disable PWM4 interrupt function. 1 = Enable PWM4 interrupt function.
4	EPW3	R/W	0	PWM3 interrupt control bit. 0 = Disable PWM3 interrupt function. 1 = Enable PWM3 interrupt function.
3	EPW2	R/W	0	PWM2 interrupt control bit. 0 = Disable PWM2 interrupt function. 1 = Enable PWM2 interrupt function.
2	EPW1	R/W	0	PWM1 interrupt control bit. 0 = Disable PWM1 interrupt function. 1 = Enable PWM1 interrupt function.
1..0	Reserved	R	0	

IRCON0 Register (0xA5)

Bit	Field	Type	Initial	Description
7	Reserved	R	0	
6	IE4	R/W	0	External P2.4 interrupt (INT4) request flag 0: None INT4 interrupt request. 1: INT4 interrupt request.
5	IE3	R/W	0	External P2.3 interrupt (INT3) request flag 0: None INT3 interrupt request.

				1: INT3 interrupt request.
4	IE2	R/W	0	External P2.2 interrupt (INT2) request flag 0: None INT2 interrupt request. 1: INT2 interrupt request.
3..0	Reserved	R	0	

IRCON2 Register (0xA7)

Bit	Field	Type	Initial	Description
7..3	Reserved	R	0	
2	TF2	R/W	0	Timer 2 interrupt request flag. 0: None T2 interrupt request 1: T2 interrupt request.
1	ADCF	R/W	0	ADC interrupt request flag. 0: None ADC interrupt request. 1: ADC interrupt request.
0	LVDF	R/W	0	LVD interrupt request flag. 0: None LVD interrupt request. 1: LVD interrupt request.

IRCON3 Register (0xED)

Bit	Field	Type	Initial	Description
7	TF4	R/W	0	Timer 4 interrupt request flag. 0: None T4 interrupt request 1: T4 interrupt request.
6	TF3	R/W	0	Timer 3 interrupt request flag. 0: None T3 interrupt request 1: T3 interrupt request.
5	PW4F	R/W	0	PWM4 interrupt request flag. 0: None PWM4 interrupt request 1: PWM4 interrupt request.
4	PW3F	R/W	0	PWM3 interrupt request flag. 0: None PWM3 interrupt request 1: PWM3 interrupt request.
3	PW2F	R/W	0	PWM2 interrupt request flag. 0: None PWM2 interrupt request 1: PWM2 interrupt request.
2	PW1F	R/W	0	PWM1 interrupt request flag.

				0: None PWM1 interrupt request 1: PWM1 interrupt request.
1..0	Reserved	R/W	0	

TCON Register (0x88)

Bit	Field	Type	Initial	Description
7	TF1	R/W	0	Timer 1 interrupt request flag. 0: None T1 interrupt request 1: T1 interrupt request.
5	TF0	R/W	0	Timer 0 interrupt request flag. 0: None T0 interrupt request 1: T0 interrupt request.
3	IE1	R/W	0	External P2.1 interrupt (INT1) request flag 0: None INT1 interrupt request. 1: INT1 interrupt request.
1	Reserved	R/W	0	
Else				Refer to other chapter(s)

S0CON Register (0x97)

Bit	Field	Type	Initial	Description
1	TI0	R/W	0	UART0 transmit interrupt request flag. It indicates completion of a serial transmission at UART0. It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software. 0: None UART0 transmit interrupt request. 1: UART0 transmit interrupt request.
0	RI0	R/W	0	UART0 receive interrupt request flag. It is set by hardware after completion of a serial reception at UART0. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes. It must be cleared by software. 0: None UART0 receive interrupt request. 1: UART0 receive interrupt request.
Else				Refer to other chapter(s)

S1CON Register (0x9C)

Bit	Field	Type	Initial	Description

1	TI1	R/W	0	UART1 transmit interrupt request flag. It indicates completion of a serial transmission at UART1. It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software. 0: None UART1 transmit interrupt request. 1: UART1 transmit interrupt request.
0	RI1	R/W	0	UART1 receive interrupt request flag. It is set by hardware after completion of a serial reception at UART1. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes. It must be cleared by software. 0: None UART1 receive interrupt request. 1: UART1 receive interrupt request.
Else				Refer to other chapter(s)

S2CON Register (0xA1)

Bit	Field	Type	Initial	Description
1	TI2	R/W	0	UART2 transmit interrupt request flag. It indicates completion of a serial transmission at UART2. It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software. 0: None UART2 transmit interrupt request. 1: UART2 transmit interrupt request.
0	RI2	R/W	0	UART2 receive interrupt request flag. It is set by hardware after completion of a serial reception at UART2. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes. It must be cleared by software. 0: None UART2 receive interrupt request. 1: UART2 receive interrupt request.
Else				Refer to other chapter(s)

I2CCON Register (0xDC)

Bit	Field	Type	Initial	Description
3	SI	R/W	0	Serial interrupt flag The SI is set by hardware when one of 25 out of 26

				possible I2C states is entered. The only state that does not set the SI is state F8h, which indicates that no relevant state information is available. The SI flag must be cleared by software. In order to clear the SI bit, '0' must be written to this bit. Writing a '1' to SI bit does not change value of the SI.
Else				Refer to other chapter(s)

SPSTA Register (0xE1)

Bit	Field	Type	Initial	Description
7	SPIF	R/W	0	Serial Peripheral Data Transfer Flag Set by hardware upon data transfer completion. Cleared by reading the SPSTA register with the SPIF bit set, and then reading the SPDAT register
4	MODF	R/W	0	Mode Fault Flag Set by hardware when the "ssn" pin level is conflict
Else				Refer to other chapter(s)

11 GPIO

The microcontroller has up to 60 bidirectional general purpose I/O pin (GPIO). Unlike the original 8051 only has open-drain output, SN8F5869 builds in push-pull output structure to improve its driving performance.

11.1 Input and Output Control

The input and output direction control is configurable through P0M to P7M registers. These bits specify each pin that is either input mode or output mode.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0M	P07M	P06M	P05M	P04M	P03M	P02M	P01M	P00M
P1M	P17M	P16M	P15M	P14M	P13M	P12M	P11M	P10M
P2M	-	-	-	P24M	P23M	P22M	P21M	P20M
P3M	P37M	P36M	P35M	P34M	P33M	P32M	P31M	P30M
P4M	P47M	P46M	P45M	P44M	P43M	P42M	P41M	P40M
P5M	P57M	P56M	P55M	P54M	P53M	P52M	P51M	P50M
P6M	P67M	P66M	P65M	P64M	P63M	P62M	P61M	P60M
P7M	P77M	P76M	P75M	P74M	P73M	P72M	P71M	P70M
ODCON	-	-	-	SPI0OD	URT3OD	URT2OD	URT1OD	URT0OD

P0M: 0xF9

Bit	Field	Type	Initial	Description
7	P07M	R/W	0	Mode selection of P0.7 0: Input mode 1: Output mode
6	P06M	R/W	0	Mode selection of P0.6 0: Input mode 1: Output mode
5	P05M	R/W	0	Mode selection of P0.5 0: Input mode 1: Output mode
4	P04M	R/W	0	Mode selection of P0.4 0: Input mode 1: Output mode
3	P03M	R/W	0	Mode selection of P0.3 0: Input mode 1: Output mode

2	P02M	R/W	0	Mode selection of P0.2 0: Input mode 1: Output mode
1	P01M	R/W	0	Mode selection of P0.1 0: Input mode 1: Output mode
0	P00M	R/W	0	Mode selection of P0.0 0: Input mode 1: Output mode

P1M: 0xFA

Bit	Field	Type	Initial	Description
7	P17M	R/W	0	*Reserved for internal testing.
6	P16M	R/W	0	Mode selection of P1.6 0: Input mode 1: Output mode
5	P15M	R/W	0	Mode selection of P1.5 0: Input mode 1: Output mode
4	P14M	R/W	0	Mode selection of P1.4 0: Input mode 1: Output mode
3	P13M	R/W	0	Mode selection of P1.3 0: Input mode 1: Output mode
2	P12M	R/W	0	Mode selection of P1.2 0: Input mode 1: Output mode
1	P11M	R/W	0	Mode selection of P1.1 0: Input mode 1: Output mode
0	P10M	R/W	0	Mode selection of P1.0 0: Input mode 1: Output mode

P2M: 0xFB

Bit	Field	Type	Initial	Description
Else	Reserved	R	0	
4	P24M	R/W	0	Mode selection of P2.4 0: Input mode 1: Output mode
3	P23M	R/W	0	Mode selection of P2.3 0: Input mode 1: Output mode
2	P22M	R/W	0	Mode selection of P2.2 0: Input mode 1: Output mode
1	P21M	R/W	0	Mode selection of P2.1 0: Input mode 1: Output mode
0	P20M	R/W	0	*Reserved for internal testing.

P3M: 0xFC

Bit	Field	Type	Initial	Description
7	P37M	R/W	0	Mode selection of P3.7 0: Input mode 1: Output mode
6	P36M	R/W	0	Mode selection of P3.6 0: Input mode 1: Output mode
5	P35M	R/W	0	Mode selection of P3.5 0: Input mode 1: Output mode
4	P34M	R/W	0	Mode selection of P3.4 0: Input mode 1: Output mode
3	P33M	R/W	0	Mode selection of P3.3 0: Input mode 1: Output mode
2	P32M	R/W	0	Mode selection of P3.2 0: Input mode

				1: Output mode
1	P31M	R/W	0	Mode selection of P3.1 0: Input mode 1: Output mode
0	P30M	R/W	0	Mode selection of P3.0 0: Input mode 1: Output mode

P4M: 0xFD

Bit	Field	Type	Initial	Description
7	P47M	R/W	0	Mode selection of P4.7 0: Input mode 1: Output mode
6	P46M	R/W	0	Mode selection of P4.6 0: Input mode 1: Output mode
5	P45M	R/W	0	Mode selection of P4.5 0: Input mode 1: Output mode
4	P44M	R/W	0	Mode selection of P4.4 0: Input mode 1: Output mode
3	P43M	R/W	0	Mode selection of P4.3 0: Input mode 1: Output mode
2	P42M	R/W	0	Mode selection of P4.2 0: Input mode 1: Output mode
1	P41M	R/W	0	Mode selection of P4.1 0: Input mode 1: Output mode
0	P40M	R/W	0	Mode selection of P4.0 0: Input mode 1: Output mode

P5M: 0xFE

Bit	Field	Type	Initial	Description
7	P57M	R/W	0	Mode selection of P5.7 0: Input mode 1: Output mode
6	P56M	R/W	0	Mode selection of P5.6 0: Input mode 1: Output mode
5	P55M	R/W	0	Mode selection of P5.5 0: Input mode 1: Output mode
4	P54M	R/W	0	Mode selection of P5.4 0: Input mode 1: Output mode
3	P53M	R/W	0	Mode selection of P5.3 0: Input mode 1: Output mode
2	P52M	R/W	0	Mode selection of P5.2 0: Input mode 1: Output mode
1	P51M	R/W	0	Mode selection of P5.1 0: Input mode 1: Output mode
0	P50M	R/W	0	Mode selection of P5.0 0: Input mode 1: Output mode

P6M: 0xF5

Bit	Field	Type	Initial	Description
7	P67M	R/W	0	Mode selection of P6.7 0: Input mode 1: Output mode
6	P66M	R/W	0	Mode selection of P6.6 0: Input mode 1: Output mode
5	P65M	R/W	0	Mode selection of P6.5 0: Input mode

				1: Output mode
4	P64M	R/W	0	Mode selection of P6.4 0: Input mode 1: Output mode
3	P63M	R/W	0	Mode selection of P6.3 0: Input mode 1: Output mode
2	P62M	R/W	0	Mode selection of P6.2 0: Input mode 1: Output mode
1	P61M	R/W	0	Mode selection of P6.1 0: Input mode 1: Output mode
0	P60M	R/W	0	Mode selection of P6.0 0: Input mode 1: Output mode

P7M: 0xF6

Bit	Field	Type	Initial	Description
7	P77M	R/W	0	Mode selection of P7.7 0: Input mode 1: Output mode
6	P76M	R/W	0	Mode selection of P7.6 0: Input mode 1: Output mode
5	P75M	R/W	0	Mode selection of P7.5 0: Input mode 1: Output mode
4	P74M	R/W	0	Mode selection of P7.4 0: Input mode 1: Output mode
3	P73M	R/W	0	Mode selection of P7.3 0: Input mode 1: Output mode
2	P72M	R/W	0	Mode selection of P7.2 0: Input mode 1: Output mode

1	P71M	R/W	0	Mode selection of P7.1 0: Input mode 1: Output mode
0	P70M	R/W	0	Mode selection of P7.0 0: Input mode 1: Output mode

- ***Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.***
- ***Note: P1.7 and P2.0 are not pin-out and are reserved for internal testing. Strongly recommended to set these pins as input pull-up.***

ODCON Register (0xF018)

Bit	Field	Type	Initial	Description
Else	Reserved	R	0	
4	SPI0OD	R/W	0	SPI0 open-drain control bit 0: Disable 1: Enable
3	URT3OD	R/W	0	UART3 open-drain control bit 0: Disable 1: Enable
2	URT2OD	R/W	0	UART2 open-drain control bit 0: Disable 1: Enable
1	URT1OD	R/W	0	UART1 open-drain control bit 0: Disable 1: Enable
0	URT0OD	R/W	0	UART0 open-drain control bit 0: Disable 1: Enable

11.2 Input Data and Output Data

By a read operation from any registers of P0 to P7, the current pin's logic level would be fetch to represent its external status. This operation remains functional even the pin is shared with other function like UART and I2C which can monitor the bus condition in some case.

A write P0 to P7 register value would be latched immediately, yet the value would be outputted until the mapped P0M – P7M is set to output mode. If the pin is currently in output mode, any value set to P0 to P7 register would be presented on the pin immediately.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P07	P06	P05	P04	P03	P02	P01	P00
P1	P17	P16	P15	P14	P13	P12	P11	P10
P2	-	-	-	P24	P23	P22	P21	P20
P3	P37	P36	P35	P34	P33	P32	P31	P30
P4	P47	P46	P45	P44	P43	P42	P41	P40
P5	P57	P56	P55	P54	P53	P52	P51	P50
P6	P67	P66	P65	P64	P63	P62	P61	P60
P7	P77	P76	P75	P74	P73	P72	P71	P70

P0: 0x80

Bit	Field	Type	Initial	Description
7	P07	R/W	1	Read: P0.7 pin's logic level Write 1/0: Output logic high or low (applied if P07M = 1)
6	P06	R/W	1	Read: P0.6 pin's logic level Write 1/0: Output logic high or low (applied if P06M = 1)
5	P05	R/W	1	Read: P0.5 pin's logic level Write 1/0: Output logic high or low (applied if P05M = 1)
4	P04	R/W	1	Read: P0.4 pin's logic level Write 1/0: Output logic high or low (applied if P04M = 1)
3	P03	R/W	1	Read: P0.3 pin's logic level Write 1/0: Output logic high or low (applied if P03M = 1)
2	P02	R/W	1	Read: P0.2 pin's logic level Write 1/0: Output logic high or low (applied if P02M = 1)
1	P01	R/W	1	Read: P0.1 pin's logic level Write 1/0: Output logic high or low (applied if P01M = 1)
0	P00	R/W	1	Read: P0.0 pin's logic level Write 1/0: Output logic high or low (applied if P00M = 1)

P1: 0x90

Bit	Field	Type	Initial	Description
7	P17	R/W	1	*Reserved for internal testing.
6	P16	R/W	1	Read: P1.6 pin's logic level

				Write 1/0: Output logic high or low (applied if P16M = 1)
5	P15	R/W	1	Read: P1.5 pin's logic level Write 1/0: Output logic high or low (applied if P15M = 1)
4	P14	R/W	1	Read: P1.4 pin's logic level Write 1/0: Output logic high or low (applied if P14M = 1)
3	P13	R/W	1	Read: P1.3 pin's logic level Write 1/0: Output logic high or low (applied if P13M = 1)
2	P12	R/W	1	Read: P1.2 pin's logic level Write 1/0: Output logic high or low (applied if P12M = 1)
1	P11	R/W	1	Read: P1.1 pin's logic level Write 1/0: Output logic high or low (applied if P11M = 1)
0	P10	R/W	1	Read: P1.0 pin's logic level Write 1/0: Output logic high or low (applied if P10M = 1)

P2: 0xA0

Bit	Field	Type	Initial	Description
Else	Reserved	R/W	0	
4	P24	R/W	1	Read: P2.4 pin's logic level Write 1/0: Output logic high or low (applied if P24M = 1)
3	P23	R/W	1	Read: P2.3 pin's logic level Write 1/0: Output logic high or low (applied if P23M = 1)
2	P22	R/W	1	Read: P2.2 pin's logic level Write 1/0: Output logic high or low (applied if P22M = 1)
1	P21	R/W	1	Read: P2.1 pin's logic level Write 1/0: Output logic high or low (applied if P21M = 1)
0	P20	R/W	1	*Reserved for internal testing.

P3: 0xB0

Bit	Field	Type	Initial	Description
7	P37	R/W	1	Read: P3.7 pin's logic level Write 1/0: Output logic high or low (applied if P37M = 1)
6	P36	R/W	1	Read: P3.6 pin's logic level Write 1/0: Output logic high or low (applied if P36M = 1)
5	P35	R/W	1	Read: P3.5 pin's logic level Write 1/0: Output logic high or low (applied if P35M = 1)

4	P34	R/W	1	Read: P3.4 pin's logic level Write 1/0: Output logic high or low (applied if P34M = 1)
3	P33	R/W	1	Read: P3.3 pin's logic level Write 1/0: Output logic high or low (applied if P33M = 1)
2	P32	R/W	1	Read: P3.2 pin's logic level Write 1/0: Output logic high or low (applied if P32M = 1)
1	P31	R/W	1	Read: P3.1 pin's logic level Write 1/0: Output logic high or low (applied if P31M = 1)
0	P30	R/W	1	Read: P3.0 pin's logic level Write 1/0: Output logic high or low (applied if P30M = 1)

P4: 0XC0

Bit	Field	Type	Initial	Description
7	P47	R/W	1	Read: P4.7 pin's logic level Write 1/0: Output logic high or low (applied if P47M = 1)
6	P46	R/W	1	Read: P4.6 pin's logic level Write 1/0: Output logic high or low (applied if P46M = 1)
5	P45	R/W	1	Read: P4.5 pin's logic level Write 1/0: Output logic high or low (applied if P45M = 1)
4	P44	R/W	1	Read: P4.4 pin's logic level Write 1/0: Output logic high or low (applied if P44M = 1)
3	P43	R/W	1	Read: P4.3 pin's logic level Write 1/0: Output logic high or low (applied if P43M = 1)
2	P42	R/W	1	Read: P4.2 pin's logic level Write 1/0: Output logic high or low (applied if P42M = 1)
1	P41	R/W	1	Read: P4.1 pin's logic level Write 1/0: Output logic high or low (applied if P41M = 1)
0	P40	R/W	1	Read: P4.0 pin's logic level Write 1/0: Output logic high or low (applied if P40M = 1)

P5: 0xD8

Bit	Field	Type	Initial	Description
7	P57	R/W	1	Read: P5.7 pin's logic level Write 1/0: Output logic high or low (applied if P57M = 1)
6	P56	R/W	1	Read: P5.6 pin's logic level Write 1/0: Output logic high or low (applied if P56M = 1)

5	P55	R/W	1	Read: P5.5 pin's logic level Write 1/0: Output logic high or low (applied if P55M = 1)
4	P54	R/W	1	Read: P5.4 pin's logic level Write 1/0: Output logic high or low (applied if P54M = 1)
3	P53	R/W	1	Read: P5.3 pin's logic level Write 1/0: Output logic high or low (applied if P53M = 1)
2	P52	R/W	1	Read: P5.2 pin's logic level Write 1/0: Output logic high or low (applied if P52M = 1)
1	P51	R/W	1	Read: P5.1 pin's logic level Write 1/0: Output logic high or low (applied if P51M = 1)
0	P50	R/W	1	Read: P5.0 pin's logic level Write 1/0: Output logic high or low (applied if P50M = 1)

P6: 0xE8

Bit	Field	Type	Initial	Description
7	P67	R/W	1	Read: P6.7 pin's logic level Write 1/0: Output logic high or low (applied if P67M = 1)
6	P66	R/W	1	Read: P6.6 pin's logic level Write 1/0: Output logic high or low (applied if P66M = 1)
5	P65	R/W	1	Read: P6.5 pin's logic level Write 1/0: Output logic high or low (applied if P65M = 1)
4	P64	R/W	1	Read: P6.4 pin's logic level Write 1/0: Output logic high or low (applied if P64M = 1)
3	P63	R/W	1	Read: P6.3 pin's logic level Write 1/0: Output logic high or low (applied if P63M = 1)
2	P62	R/W	1	Read: P6.2 pin's logic level Write 1/0: Output logic high or low (applied if P62M = 1)
1	P61	R/W	1	Read: P6.1 pin's logic level Write 1/0: Output logic high or low (applied if P61M = 1)
0	P60	R/W	1	Read: P6.0 pin's logic level Write 1/0: Output logic high or low (applied if P60M = 1)

P7: 0xF8

Bit	Field	Type	Initial	Description
7	P77	R/W	1	Read: P7.7 pin's logic level Write 1/0: Output logic high or low (applied if P77M = 1)

6	P76	R/W	1	Read: P7.6 pin's logic level Write 1/0: Output logic high or low (applied if P76M = 1)
5	P75	R/W	1	Read: P7.5 pin's logic level Write 1/0: Output logic high or low (applied if P75M = 1)
4	P74	R/W	1	Read: P7.4 pin's logic level Write 1/0: Output logic high or low (applied if P74M = 1)
3	P73	R/W	1	Read: P7.3 pin's logic level Write 1/0: Output logic high or low (applied if P73M = 1)
2	P72	R/W	1	Read: P7.2 pin's logic level Write 1/0: Output logic high or low (applied if P72M = 1)
1	P71	R/W	1	Read: P7.1 pin's logic level Write 1/0: Output logic high or low (applied if P71M = 1)
0	P70	R/W	1	Read: P7.0 pin's logic level Write 1/0: Output logic high or low (applied if P70M = 1)

11.3 On-chip Pull-up Resisters

The P0UR to P7UR registers are mapped to each pins' internal 100k ohm (in typical value) pull-up resister.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0UR	P07UR	P06UR	P05UR	P04UR	P03UR	P02UR	P01UR	P00UR
P1UR	P17UR	P16UR	P15UR	P14UR	P13UR	P12UR	P11UR	P10UR
P2UR	-	-	-	P24UR	P23UR	P22UR	P21UR	P20UR
P3UR	P37UR	P36UR	P35UR	P34UR	P33UR	P32UR	P31UR	P30UR
P4UR	P47UR	P46UR	P45UR	P44UR	P43UR	P42UR	P41UR	P40UR
P5UR	P57UR	P56UR	P55UR	P54UR	P53UR	P52UR	P51UR	P50UR
P6UR	P67UR	P66UR	P65UR	P64UR	P63UR	P62UR	P61UR	P60UR
P7UR	P77UR	P76UR	P75UR	P74UR	P73UR	P72UR	P71UR	P70UR

P0UR: 0xF000

Bit	Field	Type	Initial	Description
7	P07UR	R/W	0	On-chip pull-up resister control of P0.7 0: Disable* 1: Enable
6	P06UR	R/W	0	On-chip pull-up resister control of P0.6 0: Disable* 1: Enable

5	P05UR	R/W	0	On-chip pull-up resister control of P0.5 0: Disable* 1: Enable
4	P04UR	R/W	0	On-chip pull-up resister control of P0.4 0: Disable* 1: Enable
3	P03UR	R/W	0	On-chip pull-up resister control of P0.3 0: Disable* 1: Enable
2	P02UR	R/W	0	On-chip pull-up resister control of P0.2 0: Disable* 1: Enable
1	P01UR	R/W	0	On-chip pull-up resister control of P0.1 0: Disable* 1: Enable
0	P00UR	R/W	0	On-chip pull-up resister control of P0.0 0: Disable* 1: Enable

* Recommended disable pull-up resister if the pin is output mode or analog function

P1UR: 0xF001

Bit	Field	Type	Initial	Description
7	P17UR	R/W	0	*Reserved for internal testing.
6	P16UR	R/W	0	On-chip pull-up resister control of P1.6 0: Disable* 1: Enable
5	P15UR	R/W	0	On-chip pull-up resister control of P1.5 0: Disable* 1: Enable
4	P14UR	R/W	0	On-chip pull-up resister control of P1.4 0: Disable* 1: Enable
3	P13UR	R/W	0	On-chip pull-up resister control of P1.3 0: Disable* 1: Enable
2	P12UR	R/W	0	On-chip pull-up resister control of P1.2 0: Disable* 1: Enable

1	P11UR	R/W	0	On-chip pull-up resister control of P1.1 0: Disable* 1: Enable
0	P10UR	R/W	0	On-chip pull-up resister control of P1.0 0: Disable* 1: Enable

* Recommended disable pull-up resister if the pin is output mode or analog function

P2UR: 0xF002

Bit	Field	Type	Initial	Description
Else	Reserved	R	0	
4	P24UR	R/W	0	On-chip pull-up resister control of P2.4 0: Disable* 1: Enable
3	P23UR	R/W	0	On-chip pull-up resister control of P2.3 0: Disable* 1: Enable
2	P22UR	R/W	0	On-chip pull-up resister control of P2.2 0: Disable* 1: Enable
1	P21UR	R/W	0	On-chip pull-up resister control of P2.1 0: Disable* 1: Enable
0	P20UR	R/W	0	*Reserved for internal testing.

* Recommended disable pull-up resister if the pin is output mode or analog function

P3UR: 0xF003

Bit	Field	Type	Initial	Description
7	P37UR	R/W	0	On-chip pull-up resister control of P3.7 0: Disable* 1: Enable
6	P36UR	R/W	0	On-chip pull-up resister control of P3.6 0: Disable* 1: Enable
5	P35UR	R/W	0	On-chip pull-up resister control of P3.5 0: Disable* 1: Enable

4	P34UR	R/W	0	On-chip pull-up resister control of P3.4 0: Disable* 1: Enable
3	P33UR	R/W	0	On-chip pull-up resister control of P3.3 0: Disable* 1: Enable
2	P32UR	R/W	0	On-chip pull-up resister control of P3.2 0: Disable* 1: Enable
1	P31UR	R/W	0	On-chip pull-up resister control of P3.1 0: Disable* 1: Enable
0	P30UR	R/W	0	On-chip pull-up resister control of P3.0 0: Disable* 1: Enable

* Recommended disable pull-up resister if the pin is output mode or analog function

P4UR: 0xF004

Bit	Field	Type	Initial	Description
7	P47UR	R/W	0	On-chip pull-up resister control of P4.7 0: Disable* 1: Enable
6	P46UR	R/W	0	On-chip pull-up resister control of P4.6 0: Disable* 1: Enable
5	P45UR	R/W	0	On-chip pull-up resister control of P4.5 0: Disable* 1: Enable
4	P44UR	R/W	0	On-chip pull-up resister control of P4.4 0: Disable* 1: Enable
3	P43UR	R/W	0	On-chip pull-up resister control of P4.3 0: Disable* 1: Enable
2	P42UR	R/W	0	On-chip pull-up resister control of P4.2 0: Disable* 1: Enable

1	P41UR	R/W	0	On-chip pull-up resister control of P4.1 0: Disable* 1: Enable
0	P40UR	R/W	0	On-chip pull-up resister control of P4.0 0: Disable* 1: Enable

* Recommended disable pull-up resister if the pin is output mode or analog function

P5UR: 0xF005

Bit	Field	Type	Initial	Description
7	P57UR	R/W	0	On-chip pull-up resister control of P5.7 0: Disable* 1: Enable
6	P56UR	R/W	0	On-chip pull-up resister control of P5.6 0: Disable* 1: Enable
5	P55UR	R/W	0	On-chip pull-up resister control of P5.5 0: Disable* 1: Enable
4	P54UR	R/W	0	On-chip pull-up resister control of P5.4 0: Disable* 1: Enable
3	P53UR	R/W	0	On-chip pull-up resister control of P5.3 0: Disable* 1: Enable
2	P52UR	R/W	0	On-chip pull-up resister control of P5.2 0: Disable* 1: Enable
1	P51UR	R/W	0	On-chip pull-up resister control of P5.1 0: Disable* 1: Enable
0	P50UR	R/W	0	On-chip pull-up resister control of P5.0 0: Disable* 1: Enable

* Recommended disable pull-up resister if the pin is output mode or analog function

P6UR: 0xF006

Bit	Field	Type	Initial	Description
7	P67UR	R/W	0	On-chip pull-up resister control of P6.7 0: Disable* 1: Enable
6	P66UR	R/W	0	On-chip pull-up resister control of P6.6 0: Disable* 1: Enable
5	P65UR	R/W	0	On-chip pull-up resister control of P6.5 0: Disable* 1: Enable
4	P64UR	R/W	0	On-chip pull-up resister control of P6.4 0: Disable* 1: Enable
3	P63UR	R/W	0	On-chip pull-up resister control of P6.3 0: Disable* 1: Enable
2	P62UR	R/W	0	On-chip pull-up resister control of P6.2 0: Disable* 1: Enable
1	P61UR	R/W	0	On-chip pull-up resister control of P6.1 0: Disable* 1: Enable
0	P60UR	R/W	0	On-chip pull-up resister control of P6.0 0: Disable* 1: Enable

* Recommended disable pull-up resister if the pin is output mode or analog function

P7UR: 0xF007

Bit	Field	Type	Initial	Description
7	P77UR	R/W	0	On-chip pull-up resister control of P7.7 0: Disable* 1: Enable
6	P76UR	R/W	0	On-chip pull-up resister control of P7.6 0: Disable* 1: Enable
5	P75UR	R/W	0	On-chip pull-up resister control of P7.5 0: Disable*

				1: Enable
4	P74UR	R/W	0	On-chip pull-up resister control of P7.4 0: Disable* 1: Enable
3	P73UR	R/W	0	On-chip pull-up resister control of P7.3 0: Disable* 1: Enable
2	P72UR	R/W	0	On-chip pull-up resister control of P7.2 0: Disable* 1: Enable
1	P71UR	R/W	0	On-chip pull-up resister control of P7.1 0: Disable* 1: Enable
0	P70UR	R/W	0	On-chip pull-up resister control of P7.0 0: Disable* 1: Enable

* Recommended disable pull-up resister if the pin is output mode or analog function

11.4 On-chip Pull-down Resisters

The P0DR to P7DR registers are mapped to each pins' internal 35k ohm (in typical value) pull-down resister.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0DR	P07DR	P06DR	P05DR	P04DR	P03DR	P02DR	P01DR	P00DR
P1DR	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
P2DR	-	-	-	P24DR	P23DR	P22DR	P21DR	P20DR
P3DR	P37DR	P36DR	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
P4DR	P47DR	P46DR	P45DR	P44DR	P43DR	P42DR	P41DR	P40DR
P5DR	P57DR	P56DR	P55DR	P54DR	P53DR	P52DR	P51DR	P50DR
P6DR	P67DR	P66DR	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR
P7DR	P77DR	P76DR	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR

P0DR: 0xF008

Bit	Field	Type	Initial	Description
7	P07DR	R/W	0	On-chip pull-down resister control of P0.7 0: Disable*

				1: Enable
6	P06DR	R/W	0	On-chip pull-down resister control of P0.6 0: Disable* 1: Enable
5	P05DR	R/W	0	On-chip pull-down resister control of P0.5 0: Disable* 1: Enable
4	P04DR	R/W	0	On-chip pull-down resister control of P0.4 0: Disable* 1: Enable
3	P03DR	R/W	0	On-chip pull-down resister control of P0.3 0: Disable* 1: Enable
2	P02DR	R/W	0	On-chip pull-down resister control of P0.2 0: Disable* 1: Enable
1	P01DR	R/W	0	On-chip pull-down resister control of P0.1 0: Disable* 1: Enable
0	P00DR	R/W	0	On-chip pull-down resister control of P0.0 0: Disable* 1: Enable

* Recommended disable pull-down resister if the pin is output mode or analog function

P1DR: 0xF009

Bit	Field	Type	Initial	Description
7	P17DR	R/W	0	*Reserved for internal testing.
6	P16DR	R/W	0	On-chip pull-down resister control of P1.6 0: Disable* 1: Enable
5	P15DR	R/W	0	On-chip pull-down resister control of P1.5 0: Disable* 1: Enable
4	P14DR	R/W	0	On-chip pull-down resister control of P1.4 0: Disable* 1: Enable
3	P13DR	R/W	0	On-chip pull-down resister control of P1.3

				0: Disable* 1: Enable
2	P12DR	R/W	0	On-chip pull-down resister control of P1.2 0: Disable* 1: Enable
1	P11DR	R/W	0	On-chip pull-down resister control of P1.1 0: Disable* 1: Enable
0	P10DR	R/W	0	On-chip pull-down resister control of P1.0 0: Disable* 1: Enable

* Recommended disable pull-down resister if the pin is output mode or analog function

P2DR: 0xF00A

Bit	Field	Type	Initial	Description
Else	Reserved	R	0	
4	P24DR	R/W	0	On-chip pull-down resister control of P2.4 0: Disable* 1: Enable
3	P23DR	R/W	0	On-chip pull-down resister control of P2.3 0: Disable* 1: Enable
2	P22DR	R/W	0	On-chip pull-down resister control of P2.2 0: Disable* 1: Enable
1	P21DR	R/W	0	On-chip pull-down resister control of P2.1 0: Disable* 1: Enable
0	P20DR	R/W	0	*Reserved for internal testing.

* Recommended disable pull-down resister if the pin is output mode or analog function

P3DR: 0xF00B

Bit	Field	Type	Initial	Description
7	P37DR	R/W	0	On-chip pull-down resister control of P3.7 0: Disable* 1: Enable
6	P36DR	R/W	0	On-chip pull-down resister control of P3.6

				0: Disable* 1: Enable
5	P35DR	R/W	0	On-chip pull-down resister control of P3.5 0: Disable* 1: Enable
4	P34DR	R/W	0	On-chip pull-down resister control of P3.4 0: Disable* 1: Enable
3	P33DR	R/W	0	On-chip pull-down resister control of P3.3 0: Disable* 1: Enable
2	P32DR	R/W	0	On-chip pull-down resister control of P3.2 0: Disable* 1: Enable
1	P31DR	R/W	0	On-chip pull-down resister control of P3.1 0: Disable* 1: Enable
0	P30DR	R/W	0	On-chip pull-down resister control of P3.0 0: Disable* 1: Enable

* Recommended disable pull-down resister if the pin is output mode or analog function

P4DR: 0xF00C

Bit	Field	Type	Initial	Description
7	P47DR	R/W	0	On-chip pull-down resister control of P4.7 0: Disable* 1: Enable
6	P46DR	R/W	0	On-chip pull-down resister control of P4.6 0: Disable* 1: Enable
5	P45DR	R/W	0	On-chip pull-down resister control of P4.5 0: Disable* 1: Enable
4	P44DR	R/W	0	On-chip pull-down resister control of P4.4 0: Disable* 1: Enable
3	P43DR	R/W	0	On-chip pull-down resister control of P4.3

				0: Disable* 1: Enable
2	P42DR	R/W	0	On-chip pull-down resister control of P4.2 0: Disable* 1: Enable
1	P41DR	R/W	0	On-chip pull-down resister control of P4.1 0: Disable* 1: Enable
0	P40DR	R/W	0	On-chip pull-down resister control of P4.0 0: Disable* 1: Enable

* Recommended disable pull-down resister if the pin is output mode or analog function

P5DR: 0xF00D

Bit	Field	Type	Initial	Description
7	P57DR	R/W	0	On-chip pull-down resister control of P5.7 0: Disable* 1: Enable
6	P56DR	R/W	0	On-chip pull-down resister control of P5.6 0: Disable* 1: Enable
5	P55DR	R/W	0	On-chip pull-down resister control of P5.5 0: Disable* 1: Enable
4	P54DR	R/W	0	On-chip pull-down resister control of P5.4 0: Disable* 1: Enable
3	P53DR	R/W	0	On-chip pull-down resister control of P5.3 0: Disable* 1: Enable
2	P52DR	R/W	0	On-chip pull-down resister control of P5.2 0: Disable* 1: Enable
1	P51DR	R/W	0	On-chip pull-down resister control of P5.1 0: Disable* 1: Enable
0	P50DR	R/W	0	On-chip pull-down resister control of P5.0

				0: Disable* 1: Enable

* Recommended disable pull-down resister if the pin is output mode or analog function

P6DR: 0xF00E

Bit	Field	Type	Initial	Description
7	P67DR	R/W	0	On-chip pull-down resister control of P6.7 0: Disable* 1: Enable
6	P66DR	R/W	0	On-chip pull-down resister control of P6.6 0: Disable* 1: Enable
5	P65DR	R/W	0	On-chip pull-down resister control of P6.5 0: Disable* 1: Enable
4	P64DR	R/W	0	On-chip pull-down resister control of P6.4 0: Disable* 1: Enable
3	P63DR	R/W	0	On-chip pull-down resister control of P6.3 0: Disable* 1: Enable
2	P62DR	R/W	0	On-chip pull-down resister control of P6.2 0: Disable* 1: Enable
1	P61DR	R/W	0	On-chip pull-down resister control of P6.1 0: Disable* 1: Enable
0	P60DR	R/W	0	On-chip pull-down resister control of P6.0 0: Disable* 1: Enable

* Recommended disable pull-down resister if the pin is output mode or analog function

P7DR: 0xF00F

Bit	Field	Type	Initial	Description
7	P77DR	R/W	0	On-chip pull-down resister control of P7.7 0: Disable* 1: Enable

6	P76DR	R/W	0	On-chip pull-down resister control of P7.6 0: Disable* 1: Enable
5	P75DR	R/W	0	On-chip pull-down resister control of P7.5 0: Disable* 1: Enable
4	P74DR	R/W	0	On-chip pull-down resister control of P7.4 0: Disable* 1: Enable
3	P73DR	R/W	0	On-chip pull-down resister control of P7.3 0: Disable* 1: Enable
2	P72DR	R/W	0	On-chip pull-down resister control of P7.2 0: Disable* 1: Enable
1	P71DR	R/W	0	On-chip pull-down resister control of P7.1 0: Disable* 1: Enable
0	P70DR	R/W	0	On-chip pull-down resister control of P7.0 0: Disable* 1: Enable

* Recommended disable pull-down resister if the pin is output mode or analog function

11.5 IO Driving strength control

The P0DRV to P7DRV registers are mapped to each pins' drive current control bit in high drive or low drive.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDRV	P7DRV	P6DRV	P5DRV	P4DRV	P3DRV	P2DRV	P1DRV	P0DRV

PDRV: 0xF01A

Bit	Field	Type	Initial	Description
7	P7DRV	R/W	1	P7 IO drive current control bit. 0: Low drive 1: High drive
6	P6DRV	R/W	1	P6 IO drive current control bit. 0: Low drive

				1: High drive
5	P5DRV	R/W	1	P5 IO drive current control bit. 0: Low drive 1: High drive
4	P4DRV	R/W	1	P4 IO drive current control bit. 0: Low drive 1: High drive
3	P3DRV	R/W	1	P3 IO drive current control bit. 0: Low drive 1: High drive
2	P2DRV	R/W	1	P2 IO drive current control bit. 0: Low drive 1: High drive
1	P1DRV	R/W	1	P1 IO drive current control bit. 0: Low drive 1: High drive
0	P0DRV	R/W	1	P0 IO drive current control bit. 0: Low drive 1: High drive

11.6 Pin Shared with Analog Function

The microcontroller builds in analog functions, such as AD and LCD. The Schmitt trigger of input channel is strongly recommended to switch off if the pin's shared analog function is enabled.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3CON	P3CON7	P3CON6	P3CON5	P3CON4	P3CON3	P3CON2	P3CON1	P3CON0
P4CON	P4CON7	P4CON6	P4CON5	P4CON4	P4CON3	P4CON2	P4CON1	P4CON0
P5CON	P5CON7	P5CON6	P5CON5	P5CON4	P5CON3	P5CON2	P5CON1	P5CON0
P6CON	P6CON7	P6CON6	P6CON5	P6CON4	P6CON3	P6CON2	P6CON1	P6CON0
P7CON	P7CON7	P7CON6	P7CON5	P7CON4	P7CON3	P7CON2	P7CON1	P7CON0

P3CON: 0xF013

Bit	Field	Type	Initial	Description
7	P3CON7	R/W	0	P3.7 configuration control bit*. 0: P3.7 can be analog input pin or digital GPIO pin. 1: P3.7 is pure analog input pin and can't be a digital GPIO pin.
6	P3CON6	R/W	0	P3.6 configuration control bit*.

				0: P3.6 can be analog input pin or digital GPIO pin. 1: P3.6 is pure analog input pin and can't be a digital GPIO pin.
5	P3CON5	R/W	0	P3.5 configuration control bit*. 0: P3.5 can be analog input pin or digital GPIO pin. 1: P3.5 is pure analog input pin and can't be a digital GPIO pin.
4	P3CON4	R/W	0	P3.4 configuration control bit*. 0: P3.4 can be analog input pin or digital GPIO pin. 1: P3.4 is pure analog input pin and can't be a digital GPIO pin.
3	P3CON3	R/W	0	P3.3 configuration control bit*. 0: P3.3 can be analog input pin or digital GPIO pin. 1: P3.3 is pure analog input pin and can't be a digital GPIO pin.
2	P3CON2	R/W	0	P3.2 configuration control bit*. 0: P3.2 can be analog input pin or digital GPIO pin. 1: P3.2 is pure analog input pin and can't be a digital GPIO pin.
1	P3CON1	R/W	0	P3.1 configuration control bit*. 0: P3.1 can be analog input pin or digital GPIO pin. 1: P3.1 is pure analog input pin and can't be a digital GPIO pin.
0	P3CON0	R/W	0	P3.0 configuration control bit*. 0: P3.0 can be analog input pin or digital GPIO pin. 1: P3.0 is pure analog input pin and can't be a digital GPIO pin.

* P3CON [7:0] will configure related Port3 pin as pure analog input pin to avoid current leakage.

P4CON: 0xF014

Bit	Field	Type	Initial	Description
7	P4CON7	R/W	0	P4.7 configuration control bit*. 0: P4.7 can be analog input pin or digital GPIO pin. 1: P4.7 is pure analog input pin and can't be a digital GPIO pin.
6	P4CON6	R/W	0	P4.6 configuration control bit*. 0: P4.6 can be analog input pin or digital GPIO pin. 1: P4.6 is pure analog input pin and can't be a digital GPIO pin.
5	P4CON5	R/W	0	P4.5 configuration control bit*. 0: P4.5 can be analog input pin or digital GPIO pin. 1: P4.5 is pure analog input pin and can't be a digital GPIO pin.
4	P4CON4	R/W	0	P4.4 configuration control bit*. 0: P4.4 can be analog input pin or digital GPIO pin. 1: P4.4 is pure analog input pin and can't be a digital GPIO pin.
3	P4CON3	R/W	0	P4.3 configuration control bit*.

				0: P4.3 can be analog input pin or digital GPIO pin. 1: P4.3 is pure analog input pin and can't be a digital GPIO pin.
2	P4CON2	R/W	0	P4.2 configuration control bit*. 0: P4.2 can be analog input pin or digital GPIO pin. 1: P4.2 is pure analog input pin and can't be a digital GPIO pin.
1	P4CON1	R/W	0	P4.1 configuration control bit*. 0: P4.1 can be analog input pin or digital GPIO pin. 1: P4.1 is pure analog input pin and can't be a digital GPIO pin.
0	P4CON0	R/W	0	P4.0 configuration control bit*. 0: P4.0 can be analog input pin or digital GPIO pin. 1: P4.0 is pure analog input pin and can't be a digital GPIO pin.

* P4CON [7:0] will configure related Port4 pin as pure analog input pin to avoid current leakage.

P5CON: 0xF015

Bit	Field	Type	Initial	Description
7	P5CON7	R/W	0	P5.7 configuration control bit*. 0: P5.7 can be analog input pin or digital GPIO pin. 1: P5.7 is pure analog input pin and can't be a digital GPIO pin.
6	P5CON6	R/W	0	P5.6 configuration control bit*. 0: P5.6 can be analog input pin or digital GPIO pin. 1: P5.6 is pure analog input pin and can't be a digital GPIO pin.
5	P5CON5	R/W	0	P5.5 configuration control bit*. 0: P5.5 can be analog input pin or digital GPIO pin. 1: P5.5 is pure analog input pin and can't be a digital GPIO pin.
4	P5CON4	R/W	0	P5.4 configuration control bit*. 0: P5.4 can be analog input pin or digital GPIO pin. 1: P5.4 is pure analog input pin and can't be a digital GPIO pin.
3	P5CON3	R/W	0	P5.3 configuration control bit*. 0: P5.3 can be analog input pin or digital GPIO pin. 1: P5.3 is pure analog input pin and can't be a digital GPIO pin.
2	P5CON2	R/W	0	P5.2 configuration control bit*. 0: P5.2 can be analog input pin or digital GPIO pin. 1: P5.2 is pure analog input pin and can't be a digital GPIO pin.
1	P5CON1	R/W	0	P5.1 configuration control bit*. 0: P5.1 can be analog input pin or digital GPIO pin. 1: P5.1 is pure analog input pin and can't be a digital GPIO pin.
0	P5CON0	R/W	0	P5.0 configuration control bit*.

				0: P5.0 can be analog input pin or digital GPIO pin. 1: P5.0 is pure analog input pin and can't be a digital GPIO pin.

* P3CON [7:0] will configure related Port3 pin as pure analog input pin to avoid current leakage.

P6CON: 0xF016

Bit	Field	Type	Initial	Description
7	P6CON7	R/W	0	P6.7 configuration control bit*. 0: P6.7 can be analog input pin or digital GPIO pin. 1: P6.7 is pure analog input pin and can't be a digital GPIO pin.
6	P6CON6	R/W	0	P6.6 configuration control bit*. 0: P6.6 can be analog input pin or digital GPIO pin. 1: P6.6 is pure analog input pin and can't be a digital GPIO pin.
5	P6CON5	R/W	0	P6.5 configuration control bit*. 0: P6.5 can be analog input pin or digital GPIO pin. 1: P6.5 is pure analog input pin and can't be a digital GPIO pin.
4	P6CON4	R/W	0	P6.4 configuration control bit*. 0: P6.4 can be analog input pin or digital GPIO pin. 1: P6.4 is pure analog input pin and can't be a digital GPIO pin.
3	P6CON3	R/W	0	P6.3 configuration control bit*. 0: P6.3 can be analog input pin or digital GPIO pin. 1: P6.3 is pure analog input pin and can't be a digital GPIO pin.
2	P6CON2	R/W	0	P6.2 configuration control bit*. 0: P6.2 can be analog input pin or digital GPIO pin. 1: P6.2 is pure analog input pin and can't be a digital GPIO pin.
1	P6CON1	R/W	0	P6.1 configuration control bit*. 0: P6.1 can be analog input pin or digital GPIO pin. 1: P6.1 is pure analog input pin and can't be a digital GPIO pin.
0	P6CON0	R/W	0	P6.0 configuration control bit*. 0: P6.0 can be analog input pin or digital GPIO pin. 1: P6.0 is pure analog input pin and can't be a digital GPIO pin.

* P3CON [7:0] will configure related Port3 pin as pure analog input pin to avoid current leakage.

P7CON: 0xF017

Bit	Field	Type	Initial	Description
7	P7CON7	R/W	0	P7.7 configuration control bit*. 0: P7.7 can be analog input pin or digital GPIO pin. 1: P7.7 is pure analog input pin and can't be a digital GPIO pin.

6	P7CON6	R/W	0	P7.6 configuration control bit*. 0: P7.6 can be analog input pin or digital GPIO pin. 1: P7.6 is pure analog input pin and can't be a digital GPIO pin.
5	P7CON5	R/W	0	P7.5 configuration control bit*. 0: P7.5 can be analog input pin or digital GPIO pin. 1: P7.5 is pure analog input pin and can't be a digital GPIO pin.
4	P7CON4	R/W	0	P7.4 configuration control bit*. 0: P7.4 can be analog input pin or digital GPIO pin. 1: P7.4 is pure analog input pin and can't be a digital GPIO pin.
3	P7CON3	R/W	0	P7.3 configuration control bit*. 0: P7.3 can be analog input pin or digital GPIO pin. 1: P7.3 is pure analog input pin and can't be a digital GPIO pin.
2	P7CON2	R/W	0	P7.2 configuration control bit*. 0: P7.2 can be analog input pin or digital GPIO pin. 1: P7.2 is pure analog input pin and can't be a digital GPIO pin.
1	P7CON1	R/W	0	P7.1 configuration control bit*. 0: P7.1 can be analog input pin or digital GPIO pin. 1: P7.1 is pure analog input pin and can't be a digital GPIO pin.
0	P7CON0	R/W	0	P7.0 configuration control bit*. 0: P7.0 can be analog input pin or digital GPIO pin. 1: P3.0 is pure analog input pin and can't be a digital GPIO pin.

* P3CON [7:0] will configure related Port3 pin as pure analog input pin to avoid current leakage.

12 External Interrupt

INT1, INT2, INT3 and INT4 are external interrupt trigger sources. Build in edge trigger configuration function and edge direction is selected by PEDGE and PEDGE1 register. When both external interrupt (EX0/EX1/EX2/EX3/EX4) and global interrupt (EAL) are enabled, the external interrupt request flag (IE0/IE1/IE2/IE3/IE4) will be set to "1" as edge trigger event occurs. The program counter will jump to the interrupt vector (ORG 0x0003/0x0013/0x0023/0x003B/0x007B) and execute interrupt service routine. Interrupt request flag will be cleared by hardware before ISR is executed.

12.1 External Interrupt Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEDGE	EX3G1	EX3G0	EX2G1	EX2G0	EX1G1	EX1G0	EX0G1	-
PEDGE1	-	-	-	-	-	-	EX4G1	EX4G0

IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	-
TCON	TF1	TR1	TF0	TR0	IE1	-	-	-
IRCON0	-	IE4	IE3	IE2	-	-	-	-

PEDGE Register (0x8F)

Bit	Field	Type	Initial	Description
7..6	EX3G[1:0]	R/W	10	External interrupt 3 trigger edge control register. 00: Reserved. 01: Rising edge trigger. 10: Falling edge trigger (default) 11: Both rising and falling edge trigger
5..4	EX2G[1:0]	R/W	10	External interrupt 2 trigger edge control register. 00: Reserved. 01: Rising edge trigger. 10: Falling edge trigger (default) 11: Both rising and falling edge trigger
3..2	EX1G[1:0]	R/W	10	External interrupt 1 trigger edge control register. 00: Reserved. 01: Rising edge trigger. 10: Falling edge trigger (default) 11: Both rising and falling edge trigger
1..0	Reserved	R	10	11: Both rising and falling edge trigger

PEDGE1 Register (0x91)

Bit	Field	Type	Initial	Description
Else	Reserved	R	0	
1..0	EX4G[1:0]	R/W	10	External interrupt 4 trigger edge control register. 00: Reserved. 01: Rising edge trigger. 10: Falling edge trigger (default) 11: Both rising and falling edge trigger

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Enable all interrupt control bit. 0: Disable all interrupt function. 1: Enable all interrupt function.

6	EX4	R/W	0	External P2.4 interrupt (INT4) control bit. 0: Disable INT4 interrupt function. 1: Enable INT4 interrupt function.
5	EX3	R/W	0	External P2.3 interrupt (INT3) control bit. 0: Disable INT3 interrupt function. 1: Enable INT3 interrupt function.
4	EX2	R/W	0	External P2.2 interrupt (INT2) control bit. 0: Disable INT2 interrupt function. 1: Enable INT2 interrupt function.
2	EX1	R/W	0	External P2.1 interrupt (INT1) control bit. 0: Disable INT1 interrupt function. 1: Enable INT1 interrupt function.
0	Reserved	R/W	0	

TCON Register (0x88)

Bit	Field	Type	Initial	Description
3	IE1	R/W	0	External P2.1 interrupt (INT1) request flag 0: None INT1 interrupt request. 1: INT1 interrupt request.
1	Reserved	R	0	
Else				Refer to other chapter(s)

IRCON0 Register (0xA5)

Bit	Field	Type	Initial	Description
Else				Refer to other chapter(s)
6	IE4	R/W	0	External P2.4 interrupt (INT4) request flag 0: None INT4 interrupt request. 1: INT4 interrupt request.
5	IE3	R/W	0	External P2.3 interrupt (INT3) request flag 0: None INT3 interrupt request. 1: INT3 interrupt request.
4	IE2	R/W	0	External P2.2 interrupt (INT2) request flag 0: None INT2 interrupt request. 1: INT2 interrupt request.

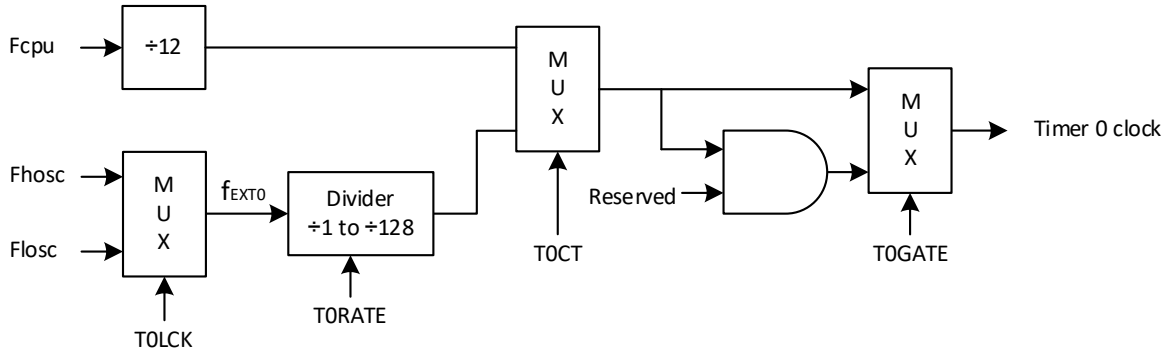
13 Timer 0 and Timer 1

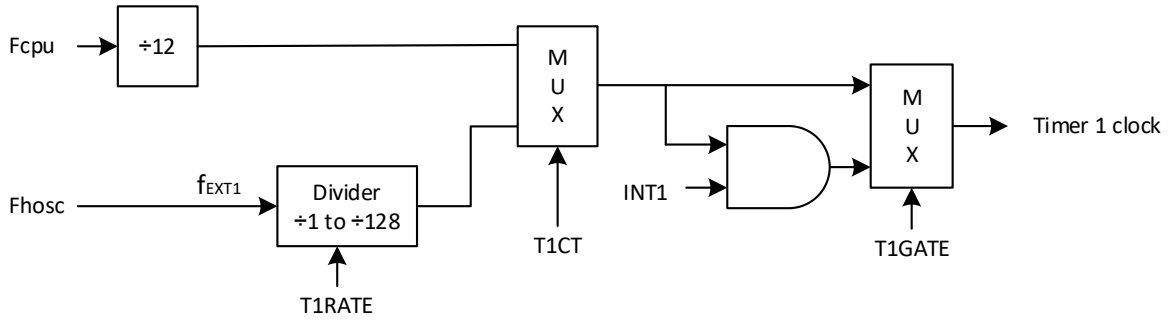
Timer 0 and Timer 1 are two independent binary up timers. Timer 0 has four different operation modes: (1) 13-bit up counting timer, (2) 16-bit up counting timer, (3) 8-bit up counting timer with specified reload value support, and (4) separated two 8-bit up counting timer. By contrast, Timer 1 has only mode 0 to mode 2 which are same as Timer 0. Timer 0 and Timer 1 respectively support ET0 and ET1 interrupt function.

When Timer 0 clock source is Flosc and STWK=1, Timer 0 can work in stop mode and waked up from stop mode by Timer 0 interrupt.

13.1 Timer 0 and Timer 1 Clock Selection

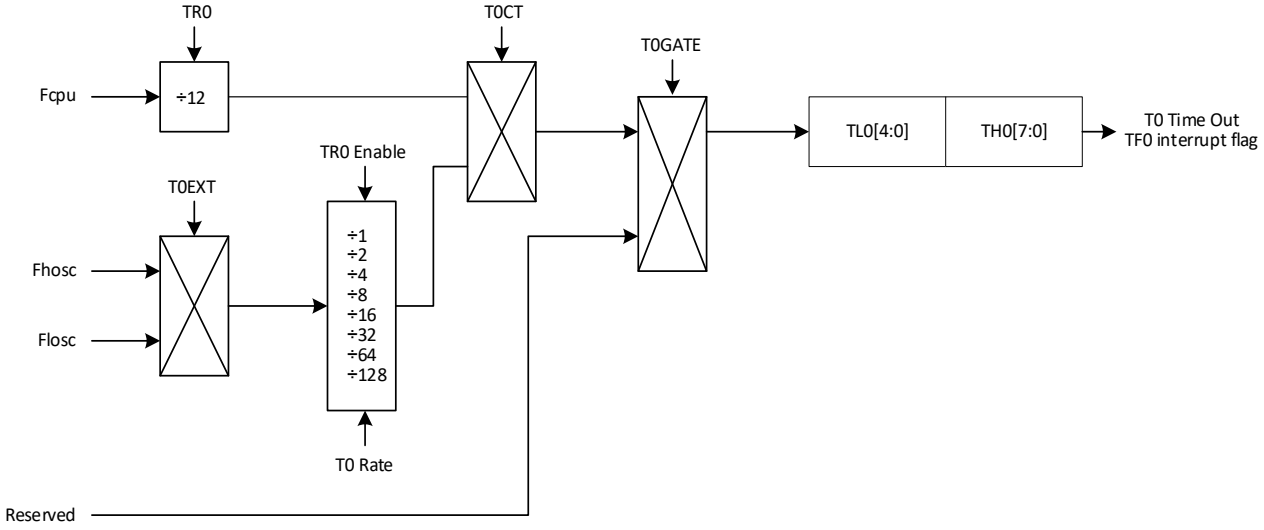
The figures below illustrate the clock selection circuit of Timer 0 and Timer 1. Timer 0 has three clock sources selection: Fcpu, Fhosc, and Flosc. All clock sources can be gated (pause) by reserved pin if T0GATE is applied. Timer 1 clock sources selection: Fcpu and Fhosc. All clock sources can be gated (pause) by INT1 pin if T1GATE is applied. Overall, the major difference between the two timers is that Timer 0 additionally supports Flosc clock source (low speed clock).

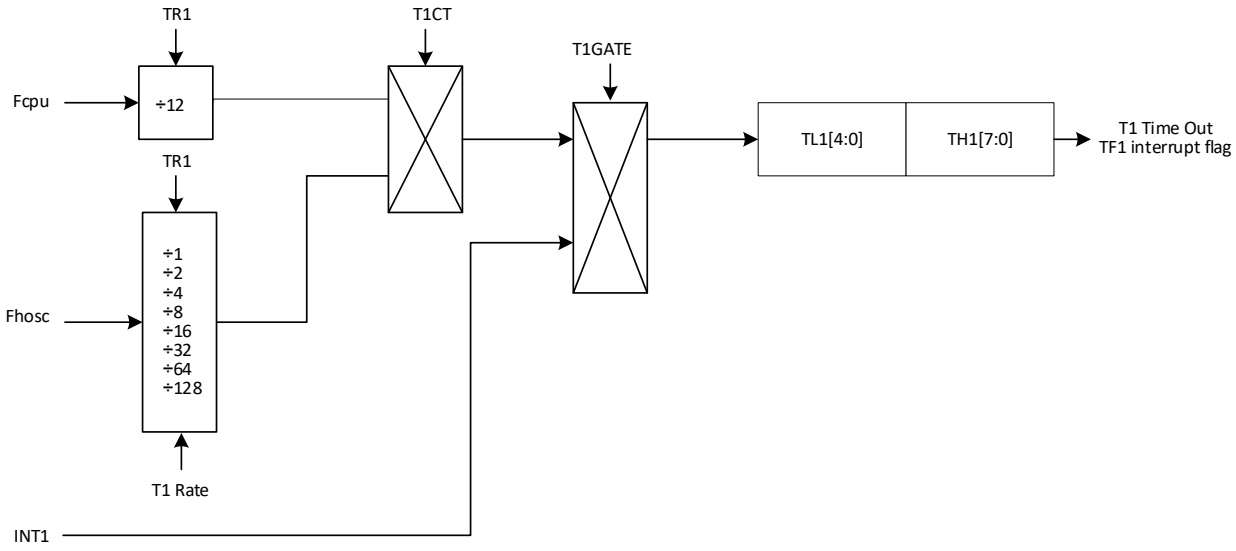




13.2 Mode 0: 13-bit Up Counting Timer

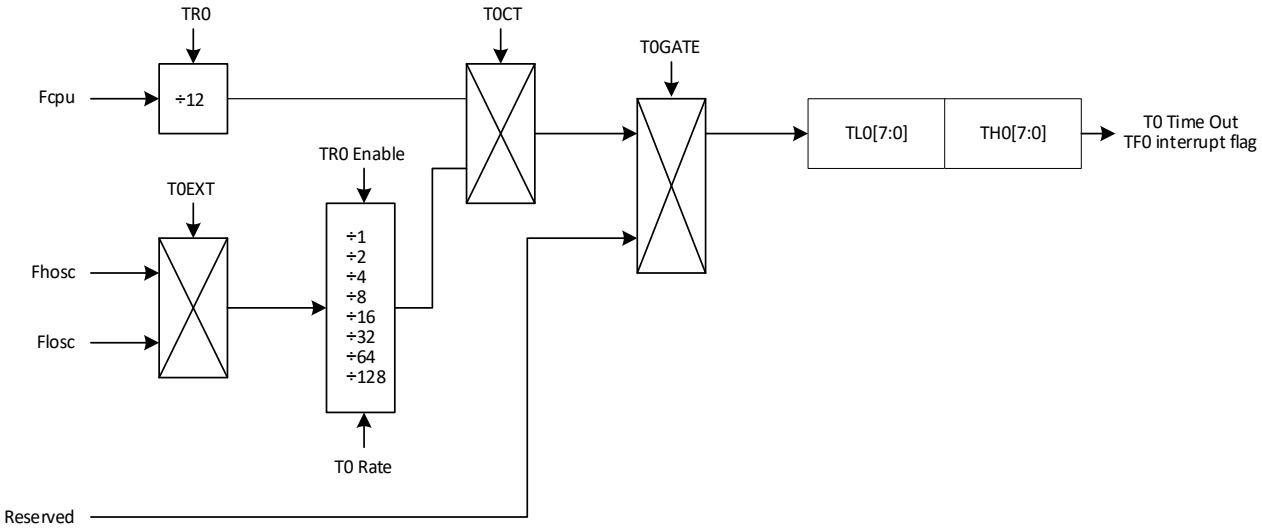
Timer 0 and Timer 1 in mode 0 is a 13-bit up counting timer (the upper 3 bits of TL0 is suspended). Once the timer's counter is overflow (counts from 0xFF1F to 0x0000), TF0/TF1 flag would be issued immediately. This flag is readable by firmware if ET0/ET1 does not apply, or can be handled by interrupt controller if ET0/ET1 is applied.

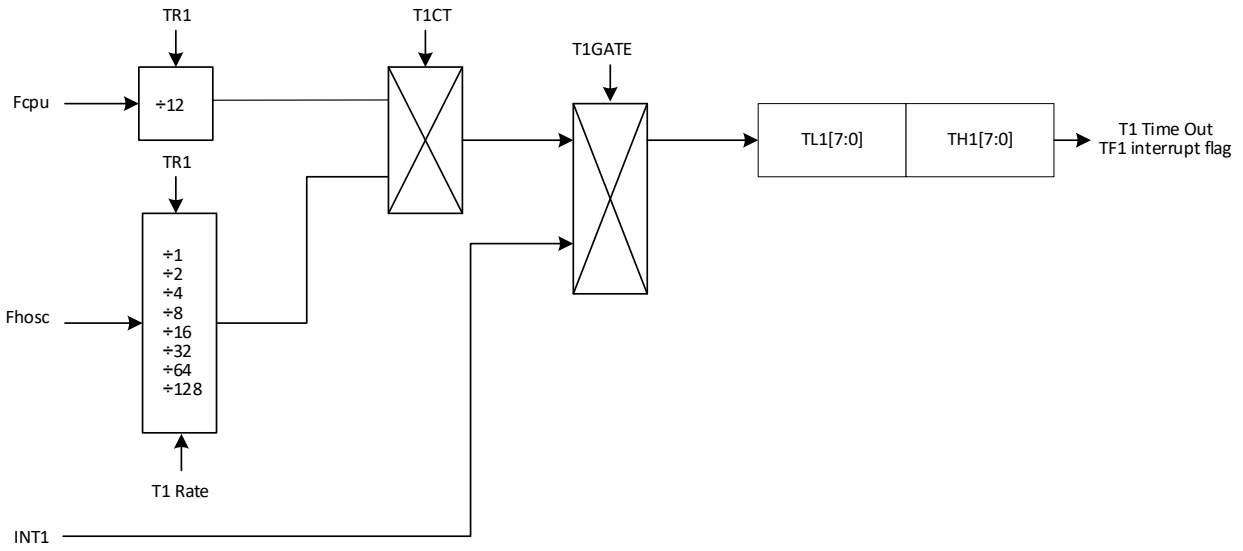




13.3 Mode 1: 16-bit Up Counting Timer

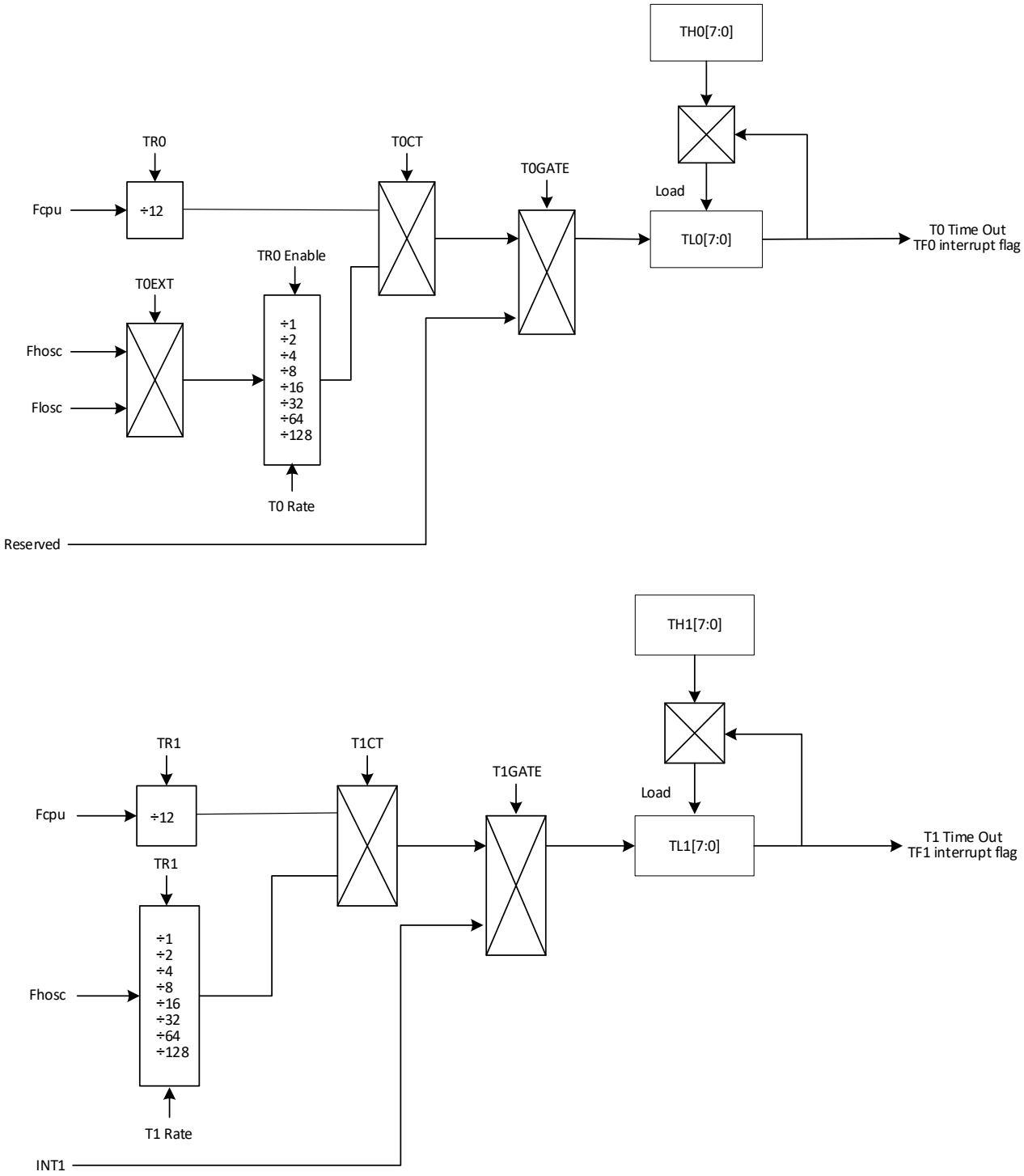
Timer 0 and Timer 1 in mode 1 is a 16-bit up counting timer. Once the timer's counter overflow is occurred (from 0xFFFF to 0x0000), TF0/TF1 would be issued which is readable by firmware or can be handled by interrupt controller (if ET0/ET1 applied).


TR0
T0CT
T0GATE
Fcpu
÷12
TR0 Enable
T0EXT
÷1
÷2
÷4
÷8
÷16
÷32
÷64
÷128
Fhosc
Flosc
TL0[7:0]
TH0[7:0]
T0 Time Out
TF0 interrupt flag
T0 Rate
Reserved


TR1
T1CT
T1GATE
Fcpu
÷12
TR1
÷1
÷2
÷4
÷8
÷16
÷32
÷64
÷128
Fhosc
TL1[7:0]
TH1[7:0]
T1 Time Out
TF1 interrupt flag
T1 Rate
INT1

13.4 Mode 2: 8-bit Up Counting Timer with Specified Reload Value Support

Timer 0 and Timer 1 in mode 2 is an 8-bit up counting timer (TL0/TL1) with a specifiable reload value. An overflow event (TL0/TL1 counts from 0xFF to 0x00) issues its TF0/TF1 flag for firmware or interrupt controller; meanwhile, the timer duplicates TH0/TH1 value to TL0/TL1 register in the same time. As a result, the timer is actually counts from 0xFF to the value of TH0/TH1.

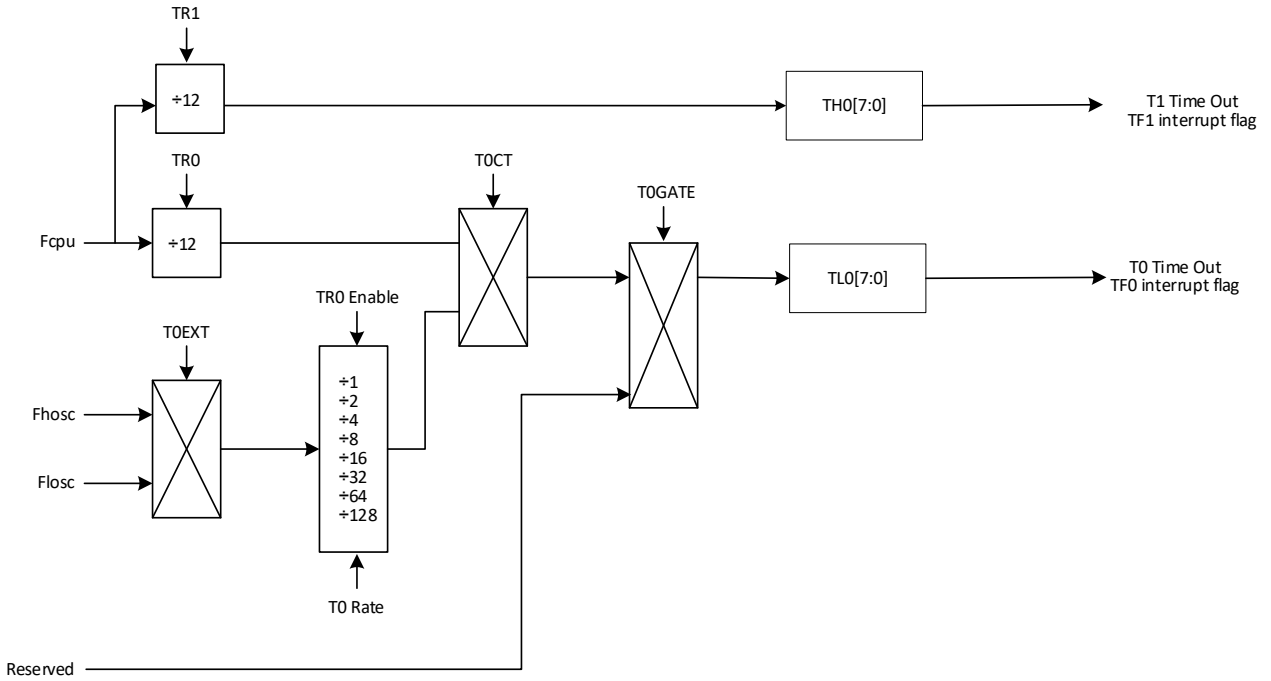


13.5 Mode 3 (Timer 0 only): Separated Two 8-bit Up Counting Timer

Mode 3 treats TH0 and TL0 as two separated 8-bit timers. TL0 is an 8-bit up counting timer with RTC support or two clock sources selection (Fcpu and Fhosc), whereas TH0 clock source is fixed at Fcpu/12. Only TL0 clock source can be gated (pause) by reserved pin if T0GATE is applied.

In this mode TL0 counter is enabled by TR0, and its overflow signal is reflected in TF0 flag. TH0 counter is controlled by TR1, and TF1 flag is also occupied by TH0 overflow signal.

Timer 1 cannot issue any overflow event in this situation, and it can be seen as a self-counting timer without flag support.



13.6 Timer 0 and Timer 1 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
TCON	TF1	TR1	TF0	TR0	IE1	-	IE0	-
TCON0	T0EXT	T0RATE2	T0RATE1	T0RATE0	-	T1RATE2	T1RATE1	T1RATE0
TMOD	T1GATE	T1CT	T1M1	T1M0	T0GATE	T0CT	T0M1	T0M0
TH0	TH07	TH06	TH05	TH04	TH03	TH02	TH01	TH00
TL0	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00
TH1	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10
TL1	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
3	ET1	R/W	0	Timer 1 interrupt 0: Disable 1: Enable
1	ET0	R/W	0	Timer 0 interrupt 0: Disable 1: Enable
Else				Refer to other chapter(s)

TH0 / TH1 Registers (TH0: 0x8C, TH1: 0x8D)

Bit	Field	Type	Initial	Description
7..0	TH0/TH1	R/W	0x00	High byte of Timer 0 and Timer 1 counter

TL0 / TL1 Register (TL0: 0x8A, TL1: 0x8B)

Bit	Field	Type	Initial	Description
7..0	TL0/TL1	R/W	0x00	Low byte of Timer 0 and Timer 1 counter

TCON Register (0x88)

Bit	Field	Type	Initial	Description
7	TF1	R/W	0	Timer 1 overflow event 0: Timer 1 does not have any overflow event 1: Timer 1 has overflowed This bit can be cleared automatically by interrupt handler, or manually by firmware
6	TR1	R/W	0	Timer 1 function 0: Disable 1: Enable
5	TF0	R/W	0	Timer 0 overflow event 0: Timer 0 does not have any overflow event 1: Timer 0 has overflowed This bit can be cleared automatically by interrupt handler, or manually by firmware
4	TR0	R/W	0	Timer 0 function 0: Disable 1: Enable
3	IE1	R/W	0	Refer to INT1
2..0	Reserved	R/W	000	

TCON0 Register (0x8E)

Bit	Field	Type	Initial	Description
7	T0EXT	R/W	0	Timer 0 f_{EXT0} clock source selection. 0: Fhosc 1: Flosc
6..4	T0RATE[2:0]	R/W	000	Clock divider of Timer 0 external clock source 000: f_{EXT0} / 128 001: f_{EXT0} / 64 010: f_{EXT0} / 32 011: f_{EXT0} / 16 100: f_{EXT0} / 8 101: f_{EXT0} / 4 110: f_{EXT0} / 2 111: f_{EXT0} / 1
3	Reserved	R	0	
2..0	T1RATE[2:0]	R/W	000	Clock divider of Timer 1 external clock source* 000: f_{EXT1} / 128 001: f_{EXT1} / 64 010: f_{EXT1} / 32 011: f_{EXT1} / 16 100: f_{EXT1} / 8 101: f_{EXT1} / 4 110: f_{EXT1} / 2 111: f_{EXT1} / 1

*(1) f_{EXT1} = Fhosc.

TMOD Register (0x89)

Bit	Field	Type	Initial	Description
7	T1GATE	R/W	0	Timer 1 gate control mode 0: Disable 1: Enable, Timer 1 clock source is gated by INT1
6	T1CT	R/W	0	Timer 1 clock source selection 0: f_{Timer1} = Fcpu / 12 1: $f_{Timer\ 1}$ = f_{EXT1} / T1RATE (refer to T1RATE) *(1)
5..4	T1M[1:0]	R/W	00	Timer 1 operation mode 00: 13-bit up counting timer 01: 16-bit up counting timer 10: 8-bit up counting timer with reload support 11: Reserved
3	T0GATE	R/W	0	Timer 0 gate control mode 0: Disable 1: Reserved
2	T0CT	R/W	0	Timer 0 clock source selection 0: f_{Timer0} = Fcpu / 12 1: f_{Timer0} = f_{EXT0} / T0RATE (refer to T0RATE) *(2)
1..0	T0M[1:0]	R/W	00	Timer 0 operation mode 00: 13-bit up counting timer 01: 16-bit up counting timer 10: 8-bit up counting timer with reload support 11: Separated two 8-bit up counting timer

*(1) f_{EXT1} = Fhosc.

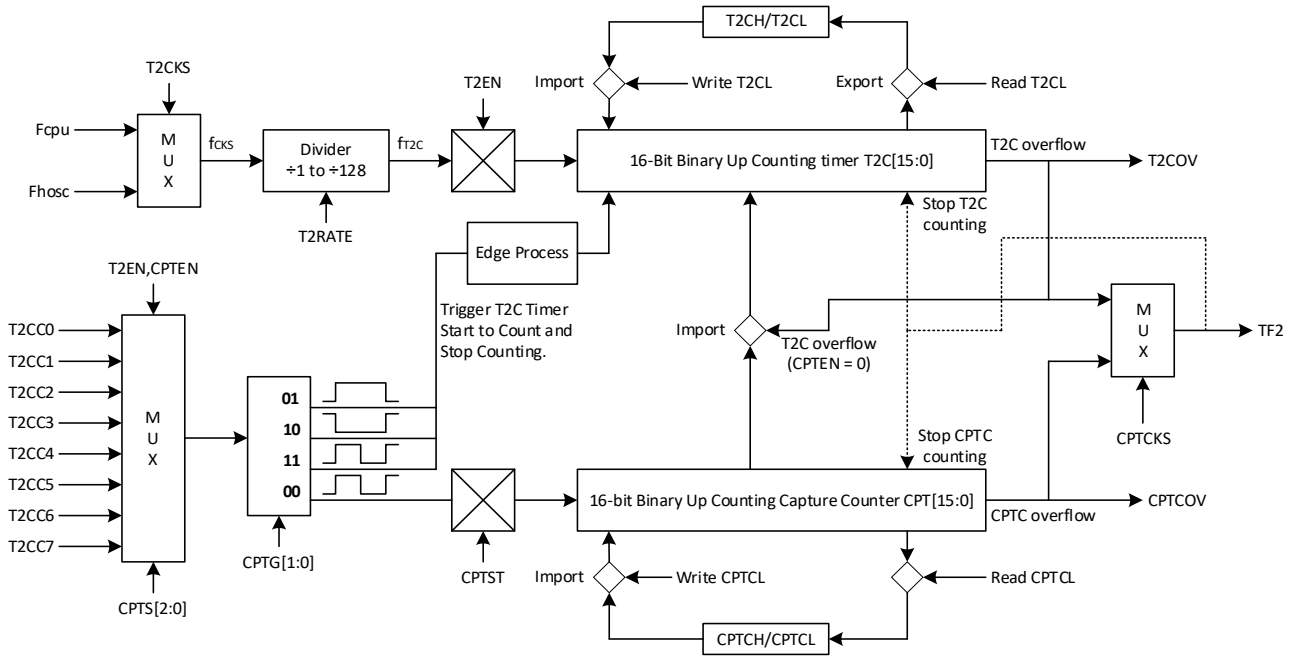
*(2) f_{EXT0} = Fhosc or Flosc.

14 Timer 2

Timer 2 includes a 16-bit binary up timer and a 16-bit binary up counter. If 16-bit timer occurs an overflow (from 0xFFFF to 0x0000) or the 16-bit counter occurs an overflow (from 0x0FFF to 0x0000), it will continue counting and issue a time-out signal to indicate Timer 2 time out event. Timer 2 can be capture timer to measure the pulse width and the cycle of input signal.

Timer 2 has six different operation modes: (1) 16-bit up counting timer with specified reload value support, (2) 16-bit low speed capture counter, (3) 16-bit high speed capture counter, (4) 16-bit high pulse width measurement counter, (5) 16-bit low pulse width measurement counter and (6) 16-bit cycle measurement counter. The measurement function have 8-input sources shared with GPIO pins and controlled by CPTS [2:0] bits.

Timer 2 builds in IDLE Mode wake-up function if interrupt enable. When timer overflow occurs or target measurement is completed, TF2 would be issued immediately which can read/write by firmware. Timer 2 interrupt function is controlled by ET2.



14.1 Timer 2 Clock Selection

The timer has two clock source options: Fcpu, Fhosc. Timer selects the clock source via the T2CKS bit and selects the frequency division by the T2RATE [2: 0] bits. The Clock division range is /1 ~ /128.

The capture timer clock source and the measurement signal are from 8-input sources: T2CC0 ~ T2CC7. The CPTC 16-bit counter is triggered on the rising edge of the input signal for up-counting. Each complete trigger signal is a cycle.

14.2 Operation Mode

Timer 2 selects six different operation modes through CPTEN, CPTMD and CPTG [1:0] bits. Each mode supports interrupt function. When timer overflow occurs or target measurement is completed, the TF2 is active and the system points program counter to interrupt vector to do interrupt sequence.

The CPTEN will determine Timer 2 is Timer mode or measurement mode. If CPTEN is Low, then Timer 2 is 16-bit up counting timer with specified reload value support. Conversely, Timer 2 can measure pulse width, cycle and capture duration of input signal. When CPTEN is high, the 16-bit up counting timer will stop for waiting measurement mode start.

The 16-bit CPTC counter is controlled by CPTEN bit, but the Timer 2 must be enabled. Set T2EN=1 and CPTEN=1 to enable capture or measurement function. The CPTC counter is a pure counter and no clock source to decide interval time.

Timer 2 can measure high pulse width, low pulse width, cycle and capture duration of input signal (T2CC0 ~ T2CC7) controlled by CPTG [1:0]. CPTST bit is to execute capture timer function. When CPTEN = 1 and CPTST is set as “1”, the T2C counter and the CPTC counter waits the right trigger edge to be activated. The trigger edge finds, and the 16-bit counter starts to count. When the second right edge finds or the capture is completed, the 16-counter will stop, CPTST is cleared and the TF2 is active.

The CPTG [1:0] bits select measurement modes: (1) 00: Capture Timer Function, (2) 01: Measure high pulse width of input pin, (3) 10: Measure low pulse width of input pin and (4) 11: Measure cycle of input pin. When measuring the pulse width or cycle of an input signal, Timer 2 uses only the T2C counter and ignores the CPTC counter.

Set CPTG [1:0] = 00 to enable capture timer function. The capture timer function’s purpose is to measure the period of a continuous signal. The function includes two modes for difference speed signal controlled by CPTMD bit. Each of overflow event occurs (controlled by CPTMD bit), the CPTC counter and T2C counter stop counting, CPTST bit is cleared, and TF2 is set as “1”.

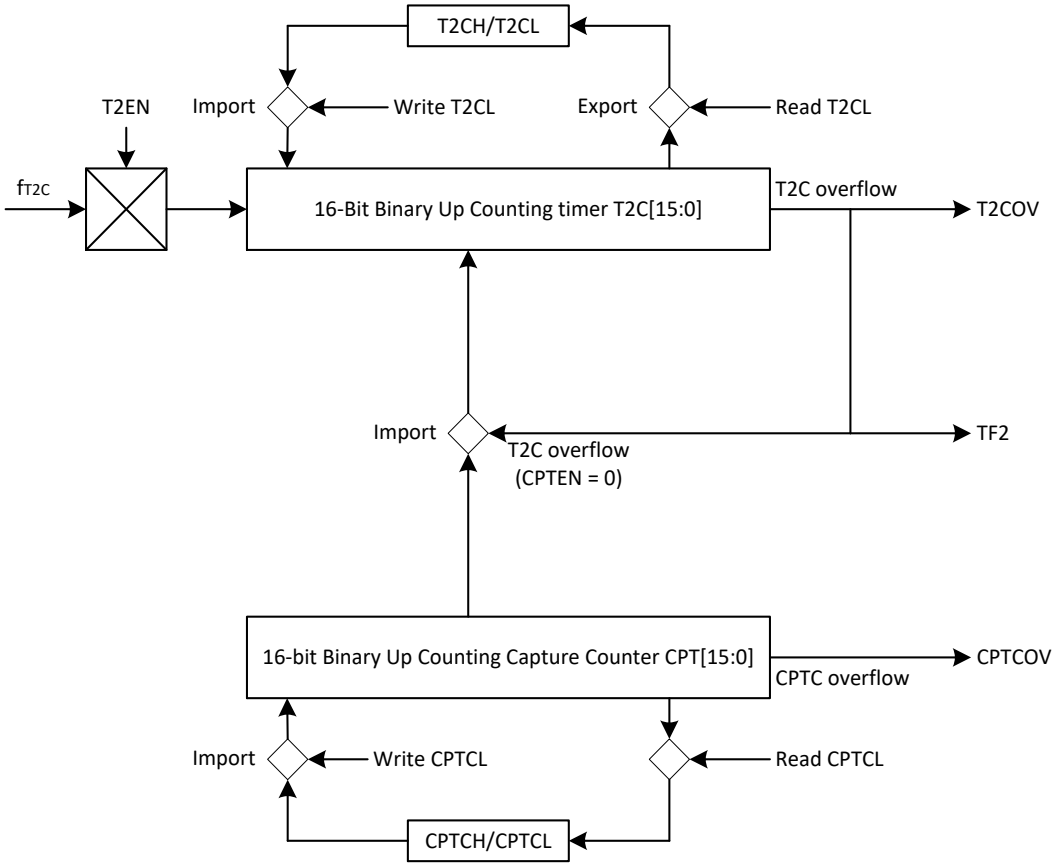
Table 14-1 The operation mode

T2EN	0	1						
CPTEN	X	0	1					
CPTST	X	X	0	1				
CPTG[1:0]	X	X	X	00		01	10	11
CPTMD	X	X	X	0	1	X	X	X
T2C[15:0]	Stop	Up counting	Stop	Timer	Timer	Timer	Timer	Timer
CPTC[15:0]	Stop	Period reload buffer	Stop	Event Counter	Event Counter	inactive	inactive	inactive
Operation mode	Inactive	Timer	Wait	Low speed capture	High speed capture	High pulse width measurement	Low pulse width measurement	Cycle measurement
Auto reload	-	Enable	-	Disable	Disable	Disable	Disable	Disable
CPTST rising edge	-	-	-	Clear T2C[15:0]	**Clear CPTC[15:0]**	Clear T2C[15:0]	Clear T2C[15:0]	Clear T2C[15:0]
T2C[15:0] Start counting	-	T2EN = 1	-	First event rising	First event rising	Event rising edge	Event falling edge	First event rising edge
T2F	inactive	T2C[15:0] overflow	-	CPTC[15:0] overflow	T2C[15:0] overflow	Event falling edge	Event rising edge	Second event rising edge
CPTST is cleared	-	-	-	CPTC[15:0] overflow	T2C[15:0] overflow	Event falling edge	Event rising edge	Second event rising edge
CPTC[15:0] overflow	-	-	-	CPTCOV = 1, T2F = 1, CPTST = 0, CPTC[15:0] & T2C[15:0] stop	**CPTCOV = 1, CPTC[15:0] & T2C[15:0] run**	-	-	-
T2C[15:0] overflow	-	T2COV = 1, T2F = 1, T2C[15:0] keep run	-	**T2COV = 1, CPTC[15:0] & T2C[15:0] keep run**	T2COV = 1, T2F = 1, CPTST = 0, CPTC[15:0] & T2C[15:0] stop	T2COV = 1, T2C[15:0] keep run	T2COV = 1, T2C[15:0] keep run	T2COV = 1, T2C[15:0] keep run

T2COV flag indicates T2CH/T2CL 16-bit timer overflow and cleared by program. CPTCOV flag indicates CPTCH/CPTCL 16-bit counter overflow and cleared by program.

14.3 Timer Mode

Timer mode is controlled by T2EN bit when CPTEN = 0. When T2EN=1, T2 timer starts to count. One count period is one clock source rate. T2C is a 16-bit binary up counter and stored in T2CH and T2CL registers. When T2C counts from 0xFFFF to 0x0000, T2 overflow condition is conformed and TF2 set as “1”. When Timer overflow occurs, the T2CH and T2CL are reload from CPTCH and CPTCL registers. T2CH and T2CL are double buffer design. If read and write T2C 16-bit counter, use read/writer T2CL to control 16-bit data latch to internal buffers. If T2 interrupt function is enabled (ET2=1), the program counter is pointed to interrupt vector to execute interrupt service routine after T2 timer overflow occurrence.

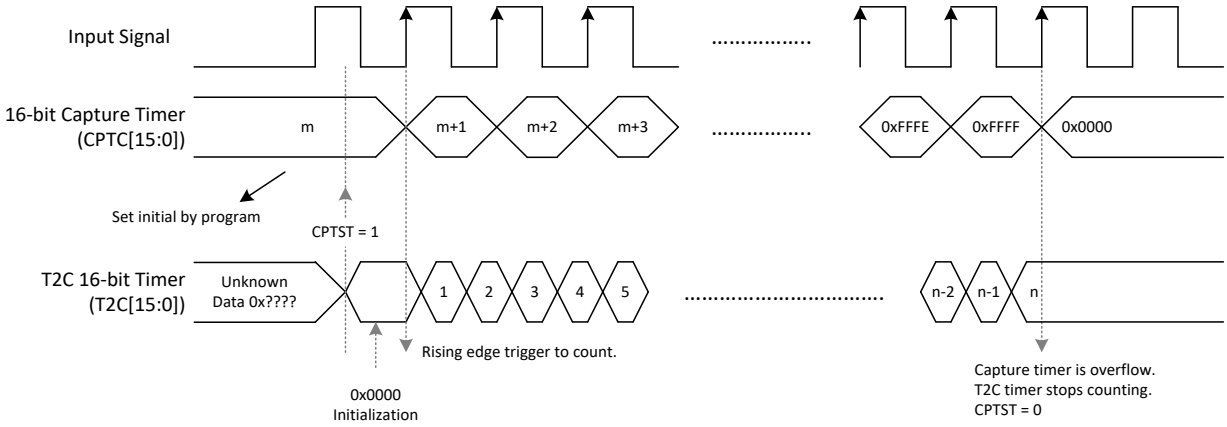


✷ ***Note:***

1. ***When CPTEN = 0, the timer reload function is enable. The timer counter reloads period value from CPTCH/CPTCL when timer counter overflow occurs.***
2. ***When CPTEN = 1, the timer reload function is disable.***

14.4 Low Speed Capture Mode

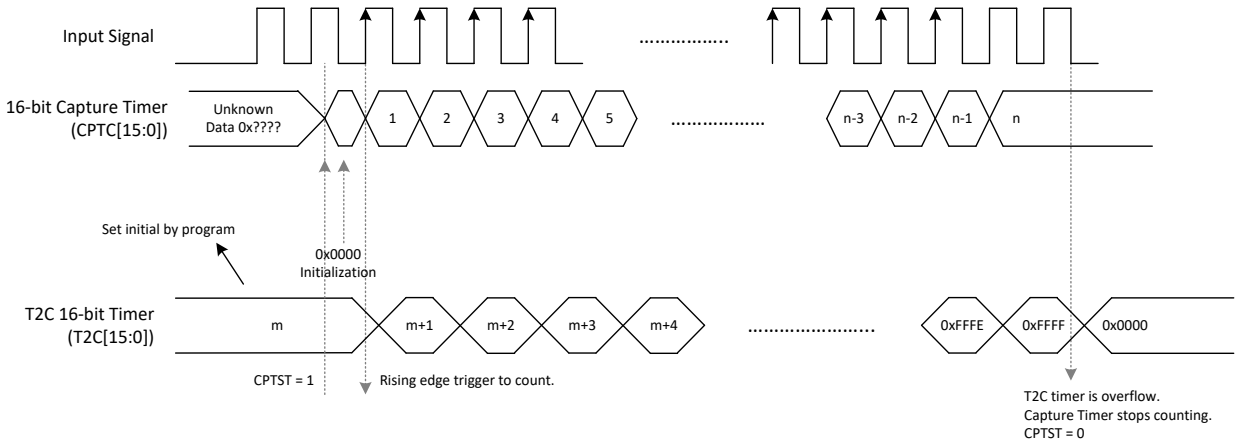
The low speed capture mode is enabled when CPTEN = 1, CPTG [1:0] = 00 and CPTMD = 0. Input signal rate < T2 timer rate. Use T2C timer to measure input signal continuous duration. Set capture timer initial value (CPTCH, CPTCL = “m”) and clear T2C timer (T2CH, T2CL = 0x0000) by program. Set CPTST bit to start capture timer counting. Capture timer and T2C timer start counting at the first rising edge of input signal. When capture timer overflow occurs (0xFFFF to 0x0000), T2C timer stops counting, CPTST is cleared automatically, and the TF2 sets as “1”. The T2C counter value (T2CH, T2CL = “n”) is the continuous signal’s duration.



✷ ***Note: When CPTST rising edge, the T2C counter will be clear.***

14.5 High Speed Capture Mode

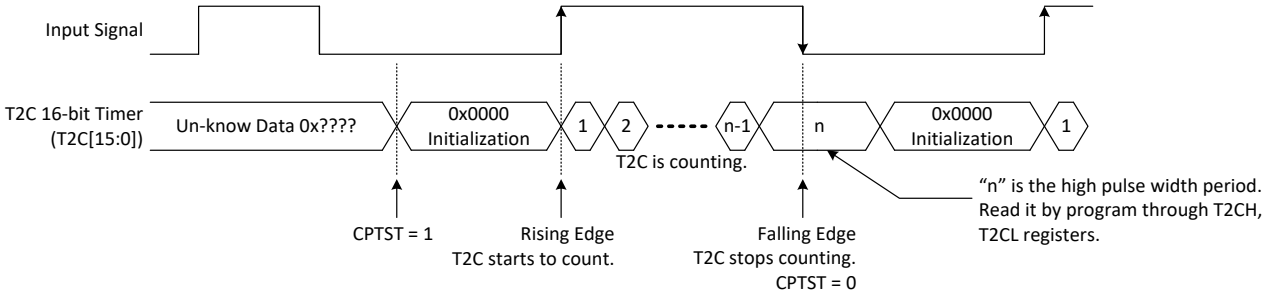
The high speed capture mode is enabled when CPTEN = 1, CPTG [1:0] = 00 and CPTMD = 1. Input signal rate > T2 timer rate. Set a unique timer by T2C timer to measure input signal counts. Set T2C timer initial value (T2CH, T2CL = “m”) and clear capture timer counter (CPTCH, CPTCL = 0x0000) by program. Set CPTST bit to start capture timer counting. Capture timer and T2C timer start counting at the first rising edge of input signal. When T2C timer overflow occurs (0xFFFF to 0x0000), capture timer stops counting, CPTST is cleared automatically, and the TF2 sets as “1”. The capture timer 16-bit counter value (CPTCH, CPTCL = “n”) is the continuous signal’s counts.



✷ ***Note: When CPTST rising edge, the capture counter will be clear.***

14.6 High Pulse Width Measurement Mode

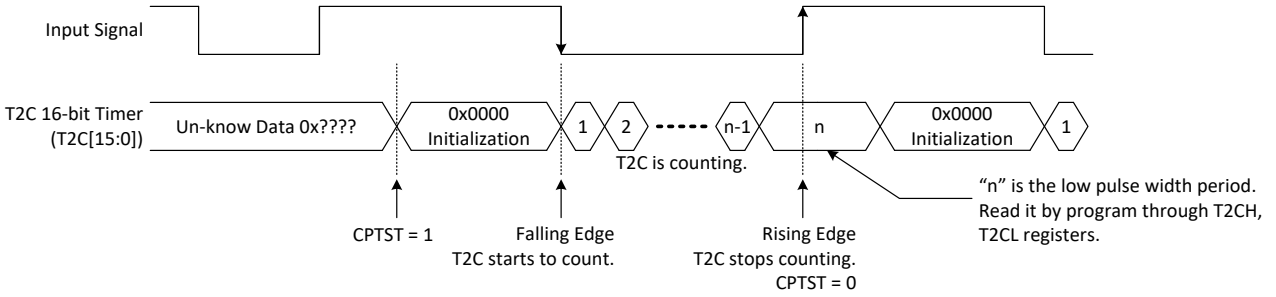
The high pulse width measurement mode is enabled when CPTEN = 1 and CPTG [1:0] = 01. The mode is using the rising edge of input signal to start T2C 16-bit timer and the falling edge of input signal to stop T2C 16-bit timer. If set CPTST bit in high pulse duration, the T2C timer will measure next high pulse until the rising edge occurrence. When the end of measuring high pulse width and T2C timer stops, the TF2 sets as "1", and the T2 interrupt executes as ET2 = 1.



✷ ***Note: When CPTST rising edge, the T2C counter will be clear.***

14.7 Low Pulse Width Measurement Mode

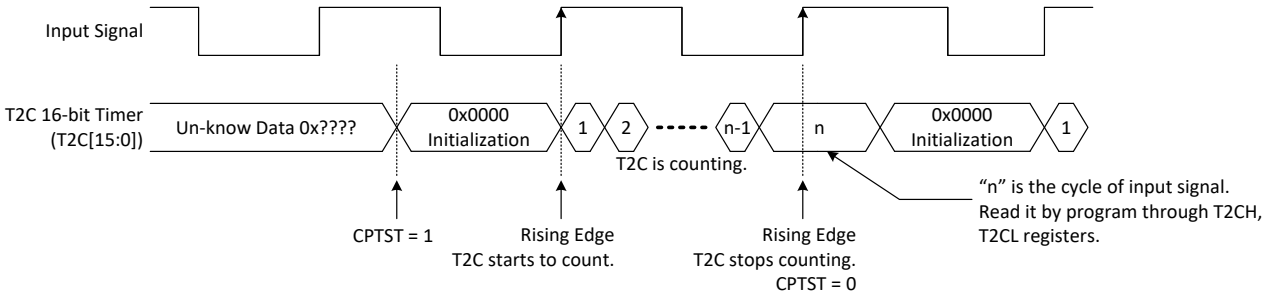
The low pulse width measurement mode is enabled when CPTEN = 1 and CPTG [1:0] = 10. The mode is using the falling edge of input signal to start T2C 16-bit timer and the rising edge of input signal to stop T2C 16-bit timer. If set CPTST bit in low pulse duration, the T2C timer will measure next low pulse until the falling edge occurrence. When the end of measuring low pulse width and T2C timer stops, the TF2 sets as "1", and the T2 interrupt executes as ET2 = 1.



✷ ***Note: When CPTST rising edge, the T2C counter will be clear.***

14.8 Cycle Measurement Mode

The cycle measurement mode is enabled when CPTEN = 1 and CPTG [1:0] = 11. The mode is using two the rising edge of input signal to start and stop T2C 16-bit timer. If set CPTST bit in high pulse duration, low pulse duration or falling edge, the T2C timer will measure next cycle until the rising edge occurrence. When the end of measuring cycle and T2C timer stops, the TF2 sets as "1", and the T2 interrupt executes as ET2 = 1.



✷ ***Note: When CPTST rising edge, the T2C counter will be clear.***

14.9 Timer 2 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2M	T2EN	T2RATE2	T2RATE1	T2RATE0	T2CKS	-	T2COV	CPTCOV
T2CH	T2C15	T2C14	T2C13	T2C12	T2C11	T2C10	T2C9	T2C8
T2CL	T2C7	T2C6	T2C5	T2C4	T2C3	T2C2	T2C1	T2C0
CPTM	CPTEN	CPTS2	CPTS1	CPTS0	CPTMD	CPTST	CPTG1	CPTG0
CPTCH	CPTC15	CPTC14	CPTC13	CPTC12	CPTC11	CPTC10	CPTC9	CPTC8
CPTCL	CPTC7	CPTC6	CPTC5	CPTC4	CPTC3	CPTC2	CPTC1	CPTC0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN2	EU3RX	EU3TX	-	-	-	ET2	EADC	ELVD
IRCON2	-	-	-	-	-	TF2	ADCF	LVDF

T2M Register (0xAC)

Bit	Field	Type	Initial	Description
7	T2EN	R/W	0	Timer 2 function enable bit 0: Disable Timer 2 module 1: Enable Timer 2 module
6..4	T2RATE[2:0]	R/W	000	Clock divider of Timer 2 f_{CKS} clock source 000: f_{CKS} / 128 001: f_{CKS} / 64 010: f_{CKS} / 32 011: f_{CKS} / 16 100: f_{CKS} / 8 101: f_{CKS} / 4 110: f_{CKS} / 2 111: f_{CKS} / 1
3	T2CKS	R/W	0	Timer 2 f_{CKS} clock source selection. 0: Fcpu 1: Fhosc
2	Reserved	R	0	
1	T2COV	R/W	0	16-bit T2C timer overflow flag 0: Non overflow 1: 16-bit timer T2C[15:0] overflows
0	CPTCOV	R/W	0	16-bit capture counter overflow flag 0: Non overflow 1: 16-bit capture counter CPTC[15:0] overflows

T2CH/T2CL Registers (T2CH: 0xB3, T2CL: 0xB2)

Bit	Field	Type	Initial	Description
7..0	T2CH/T2CL	R/W	0x00	Timer 2 16-bit timer registers. *

* Read T2 16-bit timer buffer sequence is to read T2CL first, and then read T2CH. Write T3 16-bit timer buffer sequence is to write T2CH first, and then write T2CL.

CPTM Register (0xB4)

Bit	Field	Type	Initial	Description
7	CPTEN	R/W	0	Measurement function enable bit 0: Disable 1: Enable. T2EN must be enabling.
6..4	CPTS[2:0]	R/W	0x00	Measurement function input source select bit. 000: T2CC0, 001: T2CC1, 010: T2CC2, 011: Reserved, 100: T2CC4, 101: T2CC5, 110: T2CC6, 111: T2CC7
3	CPTMD	R/W	0	Capture timer mode control bit 0: Low speed capture mode; CPTC overflow mode. 1: high speed capture mode; T2C overflow mode.
2	CPTST	R/W	0	16-bit timer and 16-bit capture counter active control bit 0: Process end 1: Start count and processing
1..0	CPTG[1:0]	R/W	00	Measurement mode select bit 00: Capture timer mode. 01: High pulse width measurement mode. 10: Low pulse width measurement mode. 11: Cycle measurement mode.

CPTCH/CPTCL Registers (CPTCH: 0xB6, CPTCL: 0xB5)

Bit	Field	Type	Initial	Description
7..0	CPTCH/CPTCL	R/W	0x00	Timer 2 16-bit capture counter registers. *

* Read T2 16-bit timer buffer sequence is to read CPTCL first, and then read CPTCH. Write T3 16-bit timer buffer sequence is to write CPTCH first, and then write CPTCL.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt

Else				Refer to other chapter(s)

IEN2 Register (0xC8)

Bit	Field	Type	Initial	Description
2	ET2	R/W	0	Timer 2 interrupt control bit. 0: Disable 1: Enable
Else				Refer to other chapter(s)

IRCON2 Register (0xA7)

Bit	Field	Type	Initial	Description
2	TF2	R/W	0	Timer 2 overflow event or measurement is completed. 0: Timer 2 does not have any overflow event, or measurement is not completed. 1: The flag is set when timer overflow occurs or target measurement is completed. This bit can be cleared automatically by interrupt handler, or manually by firmware
Else				Refer to other chapter(s)

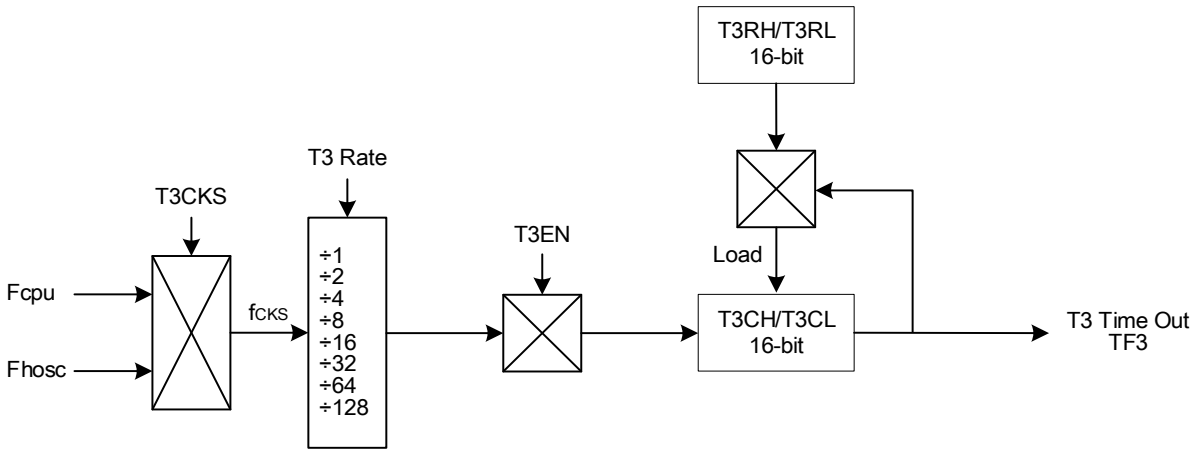
15 Timer 3

Timer 3 has 16-bit up counting timer with specified reload value support. An overflow event (T3CH/T3CL counts from 0xFFFF to 0x0000) issues its TF3 flag for firmware or interrupt controller; meanwhile, the timer duplicates T3RH/T3RL value to T3CH/T3CL register in the same time. As a result, the timer is actually counts from 0xFFFF to the value of T3RH/T3RL.

The Timer 3 build in IDLE Mode wake-up function if interrupt enable. When timer overflow occurs (counts from 0xFFFF to 0x0000), TF3 would be issued immediately which can read/write by firmware. Timer 3 interrupt function is controlled by ET3.

15.1 Timer 3 Clock Selection

Timer 3 has two clock source options: Fcpu, Fhosc. Timer 3 selects the clock source via the T3CKS bit and selects the frequency division by the T3RATE [2: 0] bits. The Clock division range is /1 ~ /128.



15.2 Timer 3 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3M	T3EN	T3RATE2	T3RATE1	T3RATE0	T3CKS	-	-	-
T3CH	T3C15	T3C14	T3C13	T3C12	T3C11	T3C10	T3C9	T3C8
T3CL	T3C7	T3C6	T3C5	T3C4	T3C3	T3C2	T3C1	T3C0
T3RH	T3R15	T3R14	T3R13	T3R12	T3R11	T3R10	T3R9	T3R8
T3RL	T3R7	T3R6	T3R5	T3R4	T3R3	T3R2	T3R1	T3R0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN3	ET4	ET3	EPW4	EPW3	EPW2	EPW1	-	-
IRCON3	TF4	TF3	PW4F	PW3F	PW2F	PW1F	-	-

T3M Register (0xF060)

Bit	Field	Type	Initial	Description
7	T3EN	R/W	0	Timer 3 function 0: Disable 1: Enable
6..4	T3RATE[2:0]	R/W	000	Clock divider of Timer 3 f_{CKS} clock source 000: f_{CKS} / 128 001: f_{CKS} / 64 010: f_{CKS} / 32 011: f_{CKS} / 16 100: f_{CKS} / 8 101: f_{CKS} / 4 110: f_{CKS} / 2 111: f_{CKS} / 1
3	T3CKS	R/W	0	Timer 3 f_{CKS} clock source selection. 0: Fcpu 1: Fhosc
2..0	Reserved	R/W	000	

T3CH/T3CL Registers (T3CH: 0xF061, T3CL: 0xF062)

Bit	Field	Type	Initial	Description
7..0	T3CH/L	R/W	0x00	16-bit Timer 3 counter buffer.

T3RH/T3RL Registers (T3RH: 0xF063, T3RL: 0xF064)

Bit	Field	Type	Initial	Description
7..0	T3RH/L	R/W	0x00	16-bit Timer 3 counter reload buffer.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN3 Register (0xEC)

Bit	Field	Type	Initial	Description
6	ET3	R/W	0	Timer 3 interrupt control bit. 0: Disable 1: Enable
Else				Refer to other chapter(s)

IRCON3 Register (0xED)

Bit	Field	Type	Initial	Description
6	TF3	R/W	0	Timer 3 overflow event 0: Timer 3 does not have any overflow event 1: Timer 3 has overflowed This bit can be cleared automatically by interrupt handler, or manually by firmware
Else				Refer to other chapter(s)

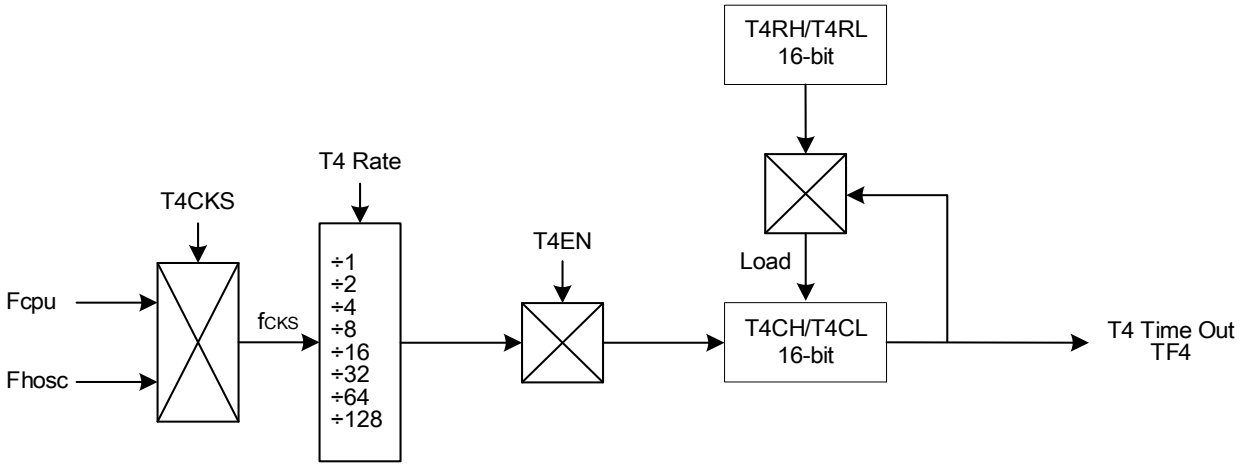
16 Timer 4

Timer 4 has 16-bit up counting timer with specified reload value support. An overflow event (T4CH/T4CL counts from 0xFFFF to 0x0000) issues its TF4 flag for firmware or interrupt controller; meanwhile, the timer duplicates T4RH/T4RL value to T4CH/T4CL register in the same time. As a result, the timer is actually counts from 0xFFFF to the value of T4RH/T4RL.

The Timer 4 build in IDLE Mode wake-up function if interrupt enable. When timer overflow occurs (counts from 0xFFFF to 0x0000), TF4 would be issued immediately which can read/write by firmware. Timer 4 interrupt function is controlled by ET4.

16.1 Timer 4 Clock Selection

Timer 4 has two clock source options: Fcpu, Fhosc. Timer 4 selects the clock source via the T4CKS bit and selects the frequency division by the T4RATE [2: 0] bits. The Clock division range is /1 ~ /128.



16.2 Timer 4 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T4M	T4EN	T4RATE2	T4RATE1	T4RATE0	T4CKS	-	-	-
T4CH	T4C15	T4C14	T4C13	T4C12	T4C11	T4C10	T4C9	T4C8
T4CL	T4C7	T4C6	T4C5	T4C4	T4C3	T4C2	T4C1	T4C0
T4RH	T4R15	T4R14	T4R13	T4R12	T4R11	T4R10	T4R9	T4R8
T4RL	T4R7	T4R6	T4R5	T4R4	T4R3	T4R2	T4R1	T4R0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN3	ET4	ET3	EPW4	EPW3	EPW2	EPW1	-	-
IRCON3	TF4	TF3	PW4F	PW3F	PW2F	PW1F	-	-

T4M Register (0xF068)

Bit	Field	Type	Initial	Description
7	T4EN	R/W	0	Timer 4 function 0: Disable 1: Enable
6..4	T4RATE[2:0]	R/W	000	Clock divider of Timer 4 f_{CKS} clock source 000: f_{CKS} / 128 001: f_{CKS} / 64 010: f_{CKS} / 32 011: f_{CKS} / 16 100: f_{CKS} / 8 101: f_{CKS} / 4 110: f_{CKS} / 2 111: f_{CKS} / 1
3	T4CKS	R/W	0	Timer 4 f_{CKS} clock source selection. 0: Fcpu 1: Fhosc
2..0	Reserved	R/W	000	

T4CH/T4CL Registers (T4CH: 0xF069, T4CL: 0xF06A)

Bit	Field	Type	Initial	Description
7..0	T4CH/L	R/W	0x00	16-bit Timer 4 counter buffer.

T4RH/T4RL Registers (T4RH: 0XF06B, T4RL: 0XF06C)

Bit	Field	Type	Initial	Description
7..0	T4RH/L	R/W	0x00	16-bit Timer 4 counter reload buffer.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN3 Register (0xEC)

Bit	Field	Type	Initial	Description
7	ET4	R/W	0	Timer 4 interrupt control bit. 0: Disable 1: Enable
Else				Refer to other chapter(s)

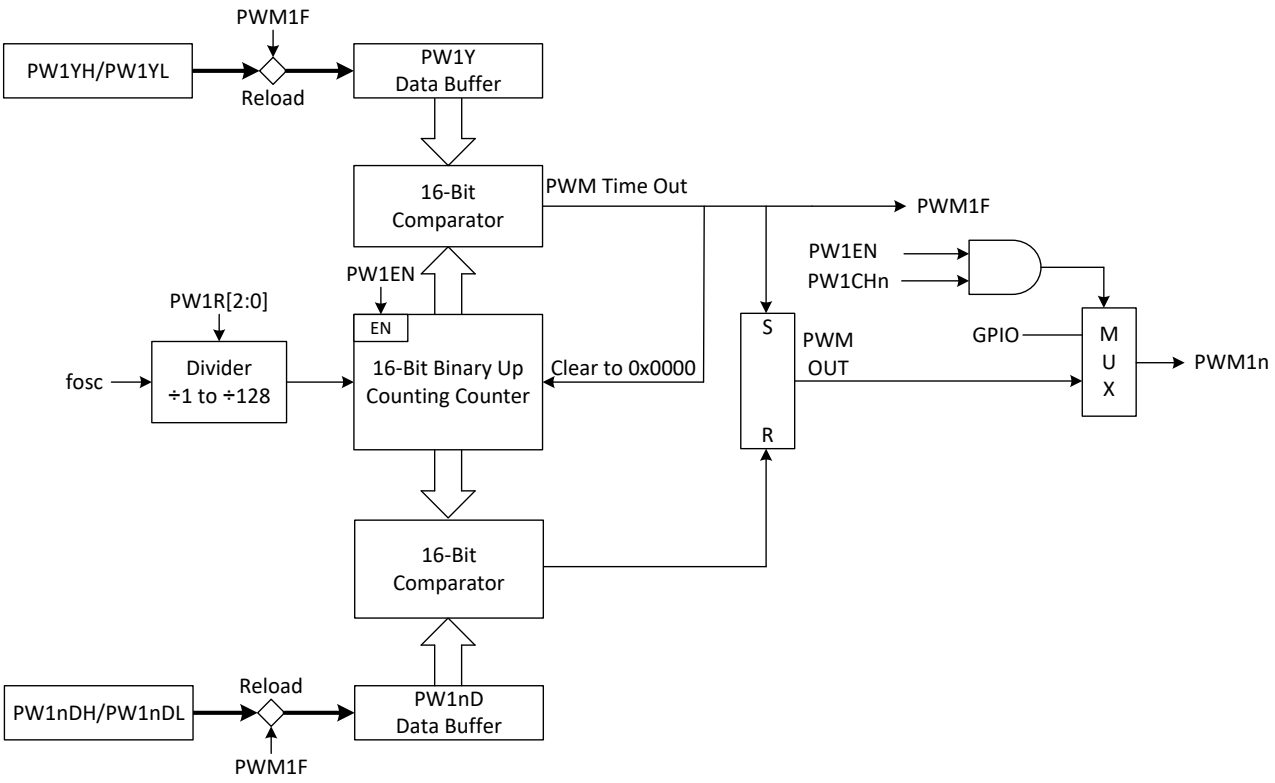
IRCON3 Register (0xED)

Bit	Field	Type	Initial	Description
7	TF4	R/W	0	Timer 4 overflow event 0: Timer 4 does not have any overflow event 1: Timer 4 has overflowed This bit can be cleared automatically by interrupt handler, or manually by firmware
Else				Refer to other chapter(s)

17 PWM1

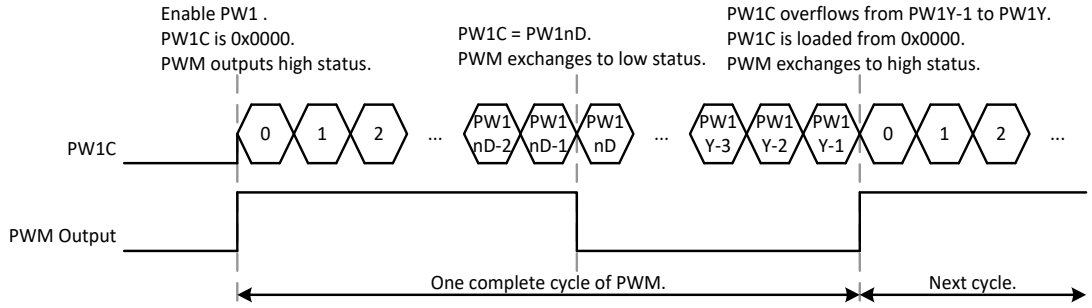
The PW1 timer is a 16-bit up counting timer and supports 4-channel general PWM function. By the counter reaches the up-boundary value PW1Y, it clears its counter and triggers an interrupt signal. PWM's duty cycle is controlled by PW10D~PW13D register. Each PWM channel has its own duty control.

The PWM function has 4 programmable channels shared with GPIO pins and controlled by PW1CH[3:0] bits. The output operation must be through enabled each bit/channel of PW1CH[3:0] bits. The enabled PWM channel exchanges from GPIO to PWM output. When the PW1CH[3:0] bits disables, the PWM channel returns to last status of GPIO mode. The PW1 timer builds in IDLE Mode wake-up function if interrupt enable. When timer overflow occurs (counts from PW1Y-1 to PW1Y), PW1F would be issued immediately which can read/write by firmware. PW1 interrupt function is controlled by EPW1.



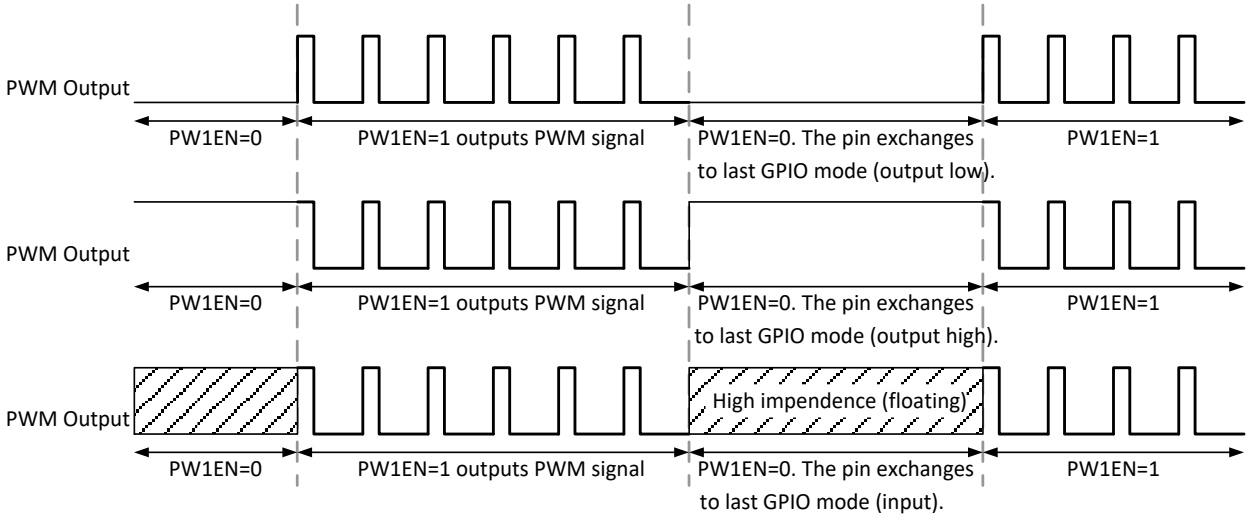
17.1 General PWM

PW1 timer builds in PWM function controlled by PW1EN register and PW1CH bits. PWM10 - PWM13 are output pins. Those output pins are shared with GPIO pin controlled by PW1CH[3:0] bits. When output PWM function, we must be set PW1EN =1. When PWM output signal synchronize finishes, the PWM channel exchanges from GPIO to PWM output. When PW1EN = 0, the PWM channel returns to GPIO mode and last status. PWM signal is generated from the result of PW1Y and PW1nD comparison combination. When PW1C starts to count or returns to 0x0000, the PWM outputs high status which is the PWM initial status. PW1C is loaded new data from PW1Y register to decide PWM cycle and resolution. PW1C keeps counting, and the system compares PW1C and PW1nD. When PW1C=PW1nD, the PWM output status exchanges to low and PW1C keeps counting. When PW1 timer overflow occurs (PW1Y-1 to 0x0000), and one cycle of PWM signal finishes. PW1C is reloaded from 0x0000 automatically, and PWM output status exchanges to high for next cycle. PW1nD decides the high duty duration, and PW1Y decides the resolution and cycle of PWM. PW1nD can't be larger than PW1Y, or the PWM signal is error. PWM clock source is Fhosc, PW1RATE[2:0] bits: 000 = Fhosc/128, 001 = Fhosc/64, 010 = Fhosc/32, 011 = Fhosc/16, 100 = Fhosc/8, 101 = Fhosc/4, 110 = Fhosc/2, 111 = Fhosc/1.



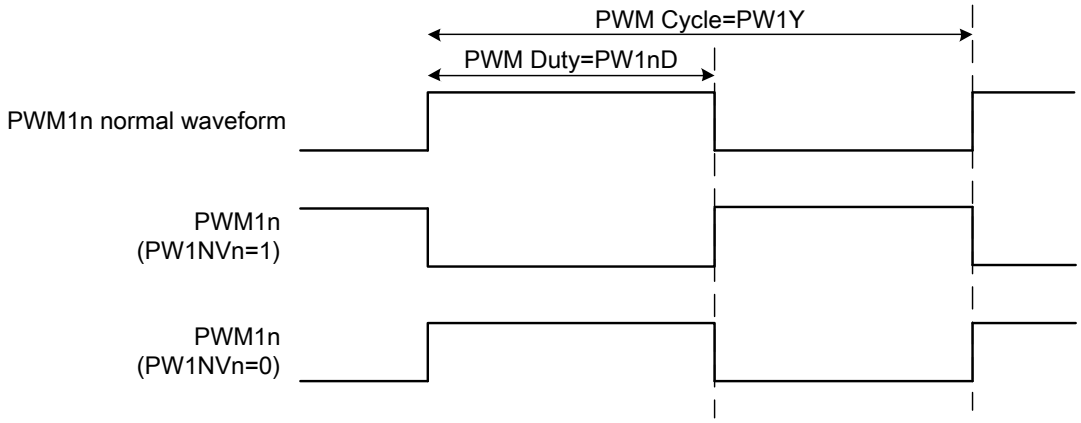
PWM Period = PW1Y

PWM duty = PW1nD/PW1Y



17.2 Inverse and Frequency Mode

The PWM builds in inverse output function. The inverse mode is controlled by PW1NV[3:0]. When PW1NVn= 1, the PWM1n outputs the inverse PWM signal of PWM. When PW1NVn = 0, the PWM1n outputs the non-inverse PWM signal of PWM. The inverse PWM output waveform is below diagram.



17.3 PWM1 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PW1M	PW1EN	PW1R2	PW1R1	PW1R0	-	-	-	-
PW1CH	-	-	-	-	PW1CH3	PW1CH2	PW1CH1	PW1CH0
PW1NV	-	-	-	-	PW1NV3	PW1NV2	PW1NV1	PW1NV0
PW1YH	PW1Y15	PW1Y14	PW1Y13	PW1Y12	PW1Y11	PW1Y10	PW1Y9	PW1Y8
PW1YL	PW1Y7	PW1Y6	PW1Y5	PW1Y4	PW1Y3	PW1Y2	PW1Y1	PW1Y0
PW10DH	PW10D15	PW10D14	PW10D13	PW10D12	PW10D11	PW10D10	PW10D9	PW10D8
PW10DL	PW10D7	PW10D6	PW10D5	PW10D4	PW10D3	PW10D2	PW10D1	PW10D0
PW11DH	PW11D15	PW11D14	PW11D13	PW11D12	PW11D11	PW11D10	PW11D9	PW11D8
PW11DL	PW11D7	PW11D6	PW11D5	PW11D4	PW11D3	PW11D2	PW11D1	PW11D0
PW12DH	PW12D15	PW12D14	PW12D13	PW12D12	PW12D11	PW12D10	PW12D9	PW12D8
PW12DL	PW12D7	PW12D6	PW12D5	PW12D4	PW12D3	PW12D2	PW12D1	PW12D0
PW13DH	PW13D15	PW13D14	PW13D13	PW13D12	PW13D11	PW13D10	PW13D9	PW13D8
PW13DL	PW13D7	PW13D6	PW13D5	PW13D4	PW13D3	PW13D2	PW13D1	PW13D0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN3	ET4	ET3	EPW4	EPW3	EPW2	EPW1	ECS	-
IRCON3	TF4	TF3	PW4F	PW3F	PW2F	PW1F	CSF	-

PW1M Register (0xF070)

Bit	Field	Type	Initial	Description
7	PW1EN	R/W	0	PW1 function 0: Disable 1: Enable*
6..4	PW1R[2:0]	R/W	000	PWM timer clock source 000: Fhosc / 128 001: Fhosc / 64 010: Fhosc / 32 011: Fhosc / 16 100: Fhosc / 8 101: Fhosc / 4 110: Fhosc / 2 111: Fhosc / 1
3..0	Reserved	R/W	0000	

* When the period is setting 0x0000, after PWM is set enable bit, the PWM will stop and the period can't update.

PW1CH Register (0xF071)

Bit	Field	Type	Initial	Description
7..4	Reserved	R/W	0000	
3	PW1CH3	R/W	0	PWM13 shared-pin control 0: GPIO 1: PWM output (shared with P1.3)
2	PW1CH2	R/W	0	PWM12 shared-pin control 0: GPIO 1: PWM output (shared with P1.2)
1	PW1CH1	R/W	0	PWM11 shared-pin control 0: GPIO 1: PWM output (shared with P1.1)
0	PW1CH0	R/W	0	PWM10 shared-pin control 0: GPIO 1: PWM output (shared with P1.0)

PW1NV Register (0xF072)

Bit	Field	Type	Initial	Description
7..4	Reserved	R/W	0000	
3	PW1NV3	R/W	0	PWM13 inverse output control

				0: PWM13 outputs non-inverse PWM signal 1: PWM13 outputs inverse PWM signal
2	PW1NV2	R/W	0	PWM12 inverse output control 0: PWM12 outputs non-inverse PWM signal 1: PWM12 outputs inverse PWM signal
1	PW1NV1	R/W	0	PWM11 inverse output control 0: PWM11 outputs non-inverse PWM signal 1: PWM11 outputs inverse PWM signal
0	PW1NV0	R/W	0	PWM10 inverse output control 0: PWM10 outputs non-inverse PWM signal 1: PWM10 outputs inverse PWM signal

PW1YH/PW1YL Registers (PW1YH: 0xF076, PW1YL: 0xF077)

Bit	Field	Type	Initial	Description
7..0	PW1YH/L	R/W	0x00	16-bit PWM1 period control*.

* The period configuration must be setup completely before starting PWM function.

PW10DH/PW10DL Registers (PW10DH: 0xF090, PW10DL: 0xF091)

Bit	Field	Type	Initial	Description
7..0	PW10DH/L	R/W	0x00	16-bit PWM1 duty control.

PW11DH/PW11DL Registers (PW11DH: 0xF092, PW11DL: 0xF093)

Bit	Field	Type	Initial	Description
7..0	PW11DH/L	R/W	0x00	16-bit PWM1 duty control.

PW12DH/PW12DL Registers (PW12DH: 0xF094, PW12DL: 0xF095)

Bit	Field	Type	Initial	Description
7..0	PW12DH/L	R/W	0x00	16-bit PWM1 duty control.

PW13DH/PW13DL Registers (PW13DH: 0xF096, PW13DL: 0xF097)

Bit	Field	Type	Initial	Description
7..0	PW13DH/L	R/W	0x00	16-bit PWM1 duty control.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN3 Register (0xEC)

Bit	Field	Type	Initial	Description
2	EPW1	R/W	0	PWM1 interrupt control bit. 0: Disable PWM1 interrupt function. 1: Enable PWM1 interrupt function.
Else				Refer to other chapter(s)

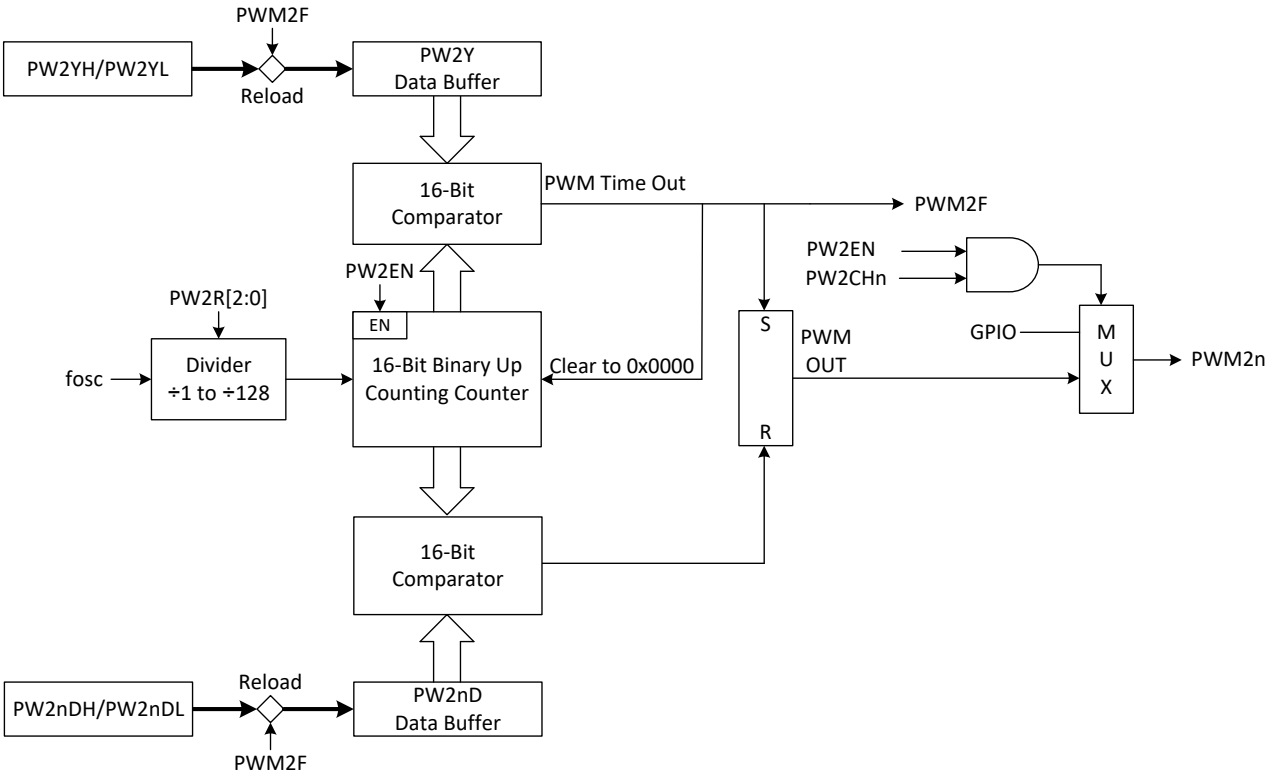
IRCON3 Register (0xED)

Bit	Field	Type	Initial	Description
2	PW1F	R/W	0	PWM1 interrupt request flag. 0: None PWM1 interrupt request 1: PWM1 interrupt request.
Else				Refer to other chapter(s)

18 PWM2

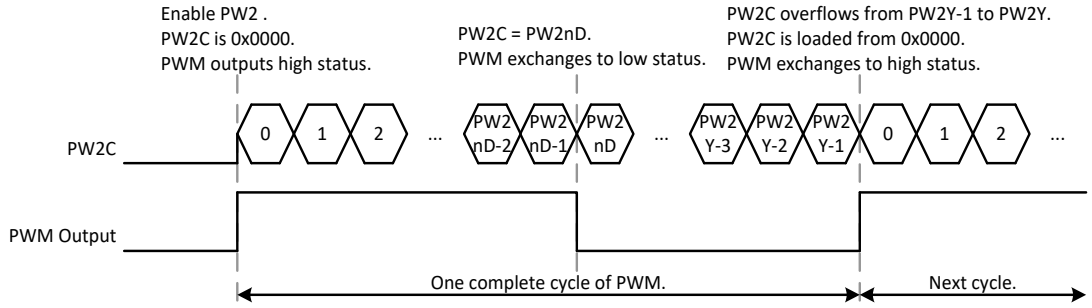
The PW2 timer is a 16-bit up counting timer and supports 4-channel general PWM function. By the counter reaches the up-boundary value PW2Y, it clears its counter and triggers an interrupt signal. PWM's duty cycle is controlled by PW20D~PW23D register. Each PWM channel has its own duty control.

The PWM function has 4 programmable channels shared with GPIO pins and controlled by PW2CH[3:0] bits. The output operation must be through enabled each bit/channel of PW2CH[3:0] bits. The enabled PWM channel exchanges from GPIO to PWM output. When the PW2CH[3:0] bits disables, the PWM channel returns to last status of GPIO mode. The PW2 timer builds in IDLE Mode wake-up function if interrupt enable. When timer overflow occurs (counts from PW2Y-1 to PW2Y), PW2F would be issued immediately which can read/write by firmware. PW2 interrupt function is controlled by EPW2.



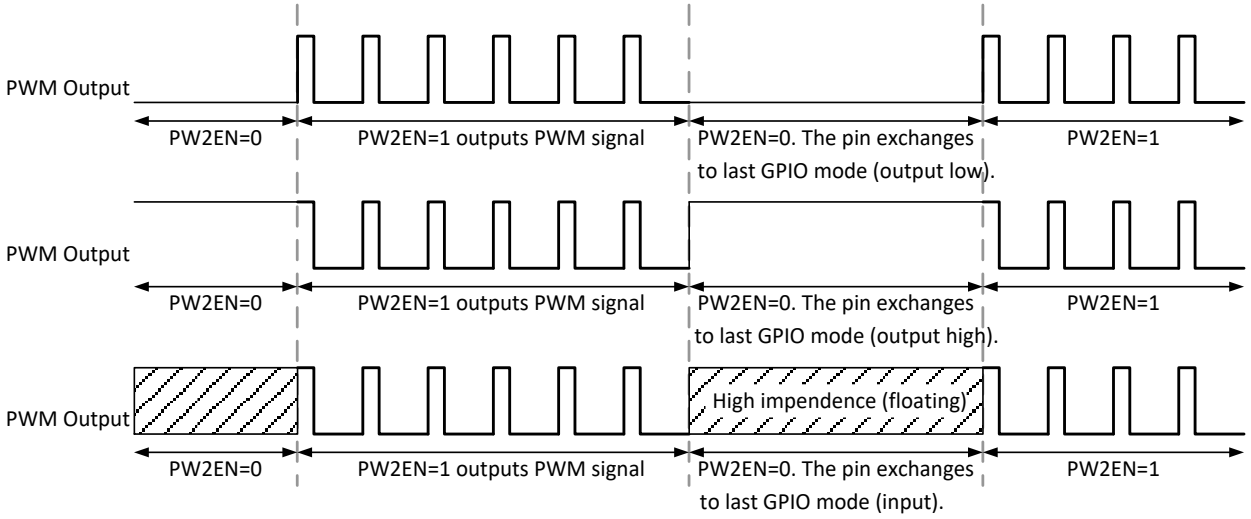
18.1 General PWM

PW2 timer builds in PWM function controlled by PW2EN register and PW2CH bits. PWM20 – PWM23 are output pins. Those output pins are shared with GPIO pin controlled by PW2CH[3:0] bits. When output PWM function, we must be set PW2EN =1. When PWM output signal synchronize finishes, the PWM channel exchanges from GPIO to PWM output. When PW2EN = 0, the PWM channel returns to GPIO mode and last status. PWM signal is generated from the result of PW2Y and PW2nD comparison combination. When PW2C starts to count or returns to 0x0000, the PWM outputs high status which is the PWM initial status. PW2C is loaded new data from PW2Y register to decide PWM cycle and resolution. PW2C keeps counting, and the system compares PW2C and PW2nD. When PW2C=PW2nD, the PWM output status exchanges to low and PW2C keeps counting. When PW2 timer overflow occurs (PW2Y-1 to 0x0000), and one cycle of PWM signal finishes. PW2C is reloaded from 0x0000 automatically, and PWM output status exchanges to high for next cycle. PW2nD decides the high duty duration, and PW2Y decides the resolution and cycle of PWM. PW2nD can't be larger than PW2Y, or the PWM signal is error. PWM clock source is Fhosc, PW2RATE[2:0] bits: 000 = Fhosc/128, 001 = Fhosc/64, 010 = Fhosc/32, 011 = Fhosc/16, 100 = Fhosc/8, 101 = Fhosc/4, 110 = Fhosc/2, 111 = Fhosc/1.



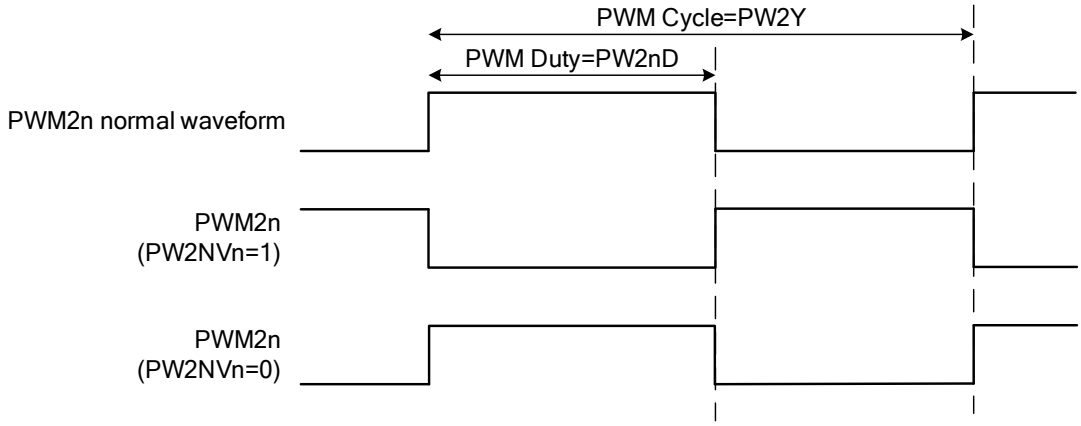
PWM Period = PW2Y

PWM duty = PW2nD/PW2Y



18.2 Inverse and Frequency Mode

The PWM builds in inverse output function. The inverse mode is controlled by PW2NV[3:0]. When PW2NVn= 1, the PWM2n outputs the inverse PWM signal of PWM. When PW2NVn = 0, the PWM2n outputs the non-inverse PWM signal of PWM. The inverse PWM output waveform is below diagram.



18.3 PWM2 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PW2M	PW2EN	PW2R2	PW2R1	PW2R0	-	-	-	-
PW2CH	-	-	-	-	PW2CH3	PW2CH2	PW2CH1	PW2CH0
PW2NV	-	-	-	-	PW2NV3	PW2NV2	PW2NV1	PW2NV0
PW2YH	PW2Y15	PW2Y14	PW2Y13	PW2Y12	PW2Y11	PW2Y10	PW2Y9	PW2Y8
PW2YL	PW2Y7	PW2Y6	PW2Y5	PW2Y4	PW2Y3	PW2Y2	PW2Y1	PW2Y0
PW20DH	PW20D15	PW20D14	PW20D13	PW20D12	PW20D11	PW20D10	PW20D9	PW20D8
PW20DL	PW20D7	PW20D6	PW20D5	PW20D4	PW20D3	PW20D2	PW20D1	PW20D0
PW21DH	PW21D15	PW21D14	PW21D13	PW21D12	PW21D11	PW21D10	PW21D9	PW21D8
PW21DL	PW21D7	PW21D6	PW21D5	PW21D4	PW21D3	PW21D2	PW21D1	PW21D0
PW22DH	PW22D15	PW22D14	PW22D13	PW22D12	PW22D11	PW22D10	PW22D9	PW22D8
PW22DL	PW22D7	PW22D6	PW22D5	PW22D4	PW22D3	PW22D2	PW22D1	PW22D0
PW23DH	PW23D15	PW23D14	PW23D13	PW23D12	PW23D11	PW23D10	PW23D9	PW23D8
PW23DL	PW23D7	PW23D6	PW23D5	PW23D4	PW23D3	PW23D2	PW23D1	PW23D0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN3	ET4	ET3	EPW4	EPW3	EPW2	EPW1	ECS	-
IRCON3	TF4	TF3	PW4F	PW3F	PW2F	PW1F	CSF	-

PW2M Register (0xF078)

Bit	Field	Type	Initial	Description

7	PW2EN	R/W	0	PW2 function 0: Disable 1: Enable*
6..4	PW2R[2:0]	R/W	000	PWM timer clock source 000: Fhosc / 128 001: Fhosc / 64 010: Fhosc / 32 011: Fhosc / 16 100: Fhosc / 8 101: Fhosc / 4 110: Fhosc / 2 111: Fhosc / 1

* When the period is setting 0x0000, after PWM is set enable bit, the PWM will stop and the period can't update.

PW2CH Register (0xF079)

Bit	Field	Type	Initial	Description
7..4	Reserved	R/W	0000	
3	PW2CH3	R/W	0	PWM23 shared-pin control 0: GPIO 1: PWM output (shared with P6.3)
2	PW2CH2	R/W	0	PWM22 shared-pin control 0: GPIO 1: PWM output (shared with P6.2)
1	PW2CH1	R/W	0	PWM21 shared-pin control 0: GPIO 1: PWM output (shared with P6.1)
0	PW2CH0	R/W	0	PWM20 shared-pin control 0: GPIO 1: PWM output (shared with P6.0)

PW2NV Register (0xF07A)

Bit	Field	Type	Initial	Description
7..4	Reserved	R/W	0000	
3	PW2NV3	R/W	0	PWM23 inverse output control 0: PWM23 outputs non-inverse PWM signal 1: PWM23 outputs inverse PWM signal
2	PW2NV2	R/W	0	PWM22 inverse output control 0: PWM22 outputs non-inverse PWM signal

				1: PWM22 outputs inverse PWM signal
1	PW2NV1	R/W	0	PWM21 inverse output control 0: PWM21 outputs non-inverse PWM signal 1: PWM21 outputs inverse PWM signal
0	PW2NV0	R/W	0	PWM20 inverse output control 0: PWM20 outputs non-inverse PWM signal 1: PWM20 outputs inverse PWM signal

PW2YH/PW2YL Registers (PW2YH: 0xF07E, PW2YL: 0xF07F)

Bit	Field	Type	Initial	Description
7..0	PW2YH/L	R/W	0x00	16-bit PWM2 period control*.

* The period configuration must be setup completely before starting PWM function.

PW20DH/PW20DL Registers (PW20DH: 0xF098, PW20DL: 0xF099)

Bit	Field	Type	Initial	Description
7..0	PW20DH/L	R/W	0x00	16-bit PWM2 duty control.

PW21DH/PW21DL Registers (PW21DH: 0xF09A, PW21DL: 0xF09B)

Bit	Field	Type	Initial	Description
7..0	PW21DH/L	R/W	0x00	16-bit PWM2 duty control.

PW22DH/PW22DL Registers (PW22DH: 0xF09C, PW22DL: 0xF09D)

Bit	Field	Type	Initial	Description
7..0	PW22DH/L	R/W	0x00	16-bit PWM2 duty control.

PW23DH/PW23DL Registers (PW23DH: 0xF09E, PW23DL: 0xF09F)

Bit	Field	Type	Initial	Description
7..0	PW23DH/L	R/W	0x00	16-bit PWM2 duty control.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN3 Register (0xEC)

Bit	Field	Type	Initial	Description

3	EPW2	R/W	0	PWM2 interrupt control bit. 0: Disable PWM2 interrupt function. 1: Enable PWM2 interrupt function.
Else				Refer to other chapter(s)

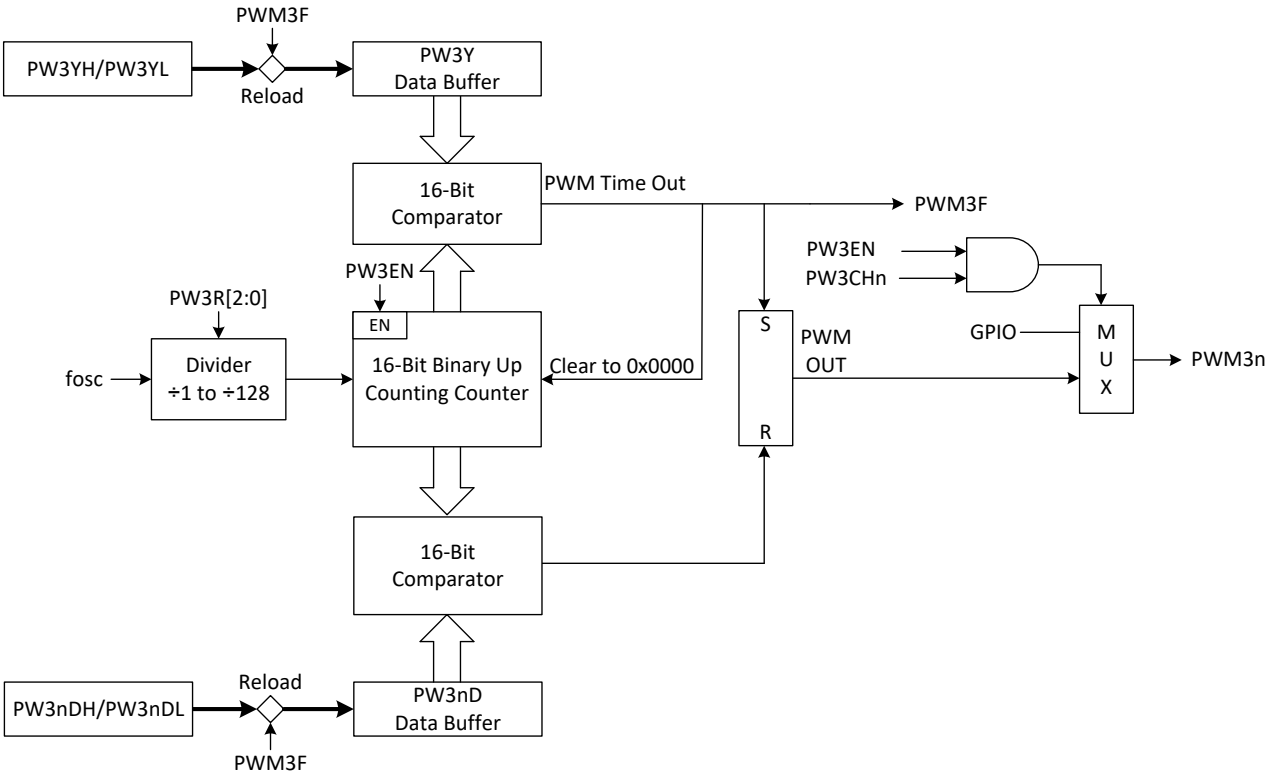
IRCON3 Register (0xED)

Bit	Field	Type	Initial	Description
3	PW2F	R/W	0	PWM2 interrupt request flag. 0: None PWM2 interrupt request 1: PWM2 interrupt request.
Else				Refer to other chapter(s)

19 PWM3

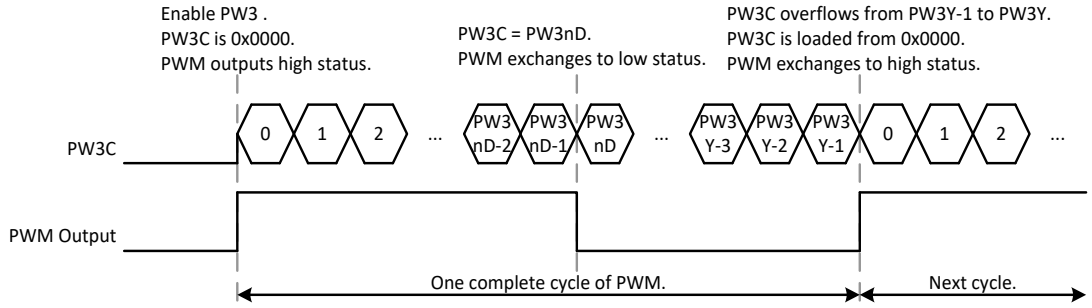
The PW3 timer is a 16-bit up counting timer and supports 3-channel general PWM function. By the counter reaches the up-boundary value PW3Y, it clears its counter and triggers an interrupt signal. PWM's duty cycle is controlled by PW30D~PW32D register. Each PWM channel has its own duty control.

The PWM function has 3 programmable channels shared with GPIO pins and controlled by PW3CH[2:0] bits. The output operation must be through enabled each bit/channel of PW3CH[2:0] bits. The enabled PWM channel exchanges from GPIO to PWM output. When the PW3CH[2:0] bits disables, the PWM channel returns to last status of GPIO mode. The PW3 timer builds in IDLE Mode wake-up function if interrupt enable. When timer overflow occurs (counts from PW3Y-1 to PW3Y), PW3F would be issued immediately which can read/write by firmware. PW3 interrupt function is controlled by EPW3.



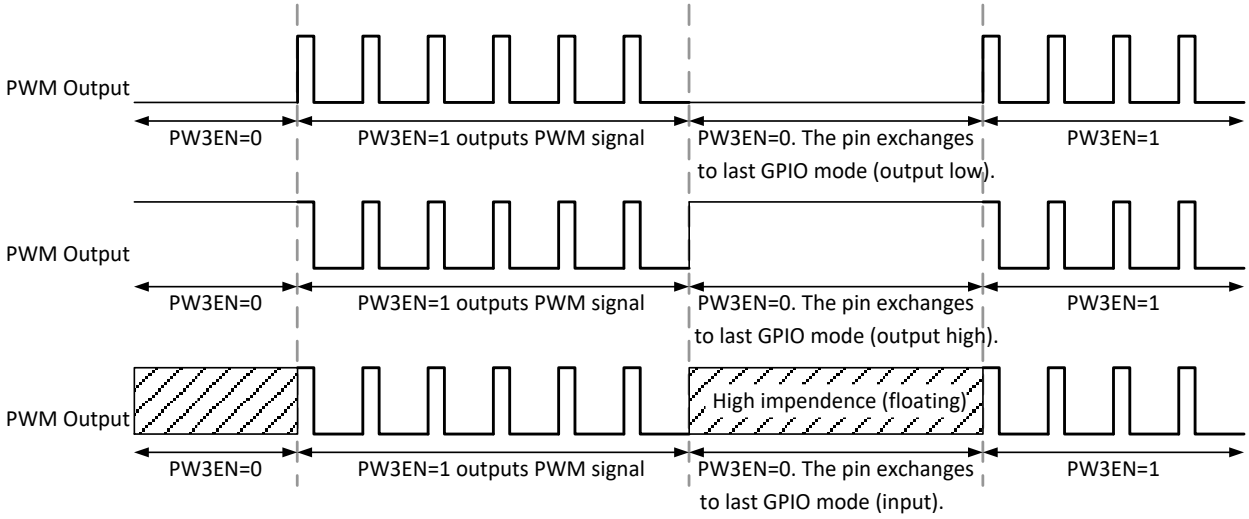
19.1 General PWM

PW3 timer builds in PWM function controlled by PW3EN register and PW3CH bits. PWM30 - PWM32 are output pins. Those output pins are shared with GPIO pin controlled by PW3CH[2:0] bits. When output PWM function, we must be set PW3EN =1. When PWM output signal synchronize finishes, the PWM channel exchanges from GPIO to PWM output. When PW3EN = 0, the PWM channel returns to GPIO mode and last status. PWM signal is generated from the result of PW3Y and PW3nD comparison combination. When PW3C starts to count or returns to 0x0000, the PWM outputs high status which is the PWM initial status. PW3C is loaded new data from PW3Y register to decide PWM cycle and resolution. PW3C keeps counting, and the system compares PW3C and PW3nD. When PW3C=PW3nD, the PWM output status exchanges to low and PW3C keeps counting. When PW3 timer overflow occurs (PW3Y-1 to 0x0000), and one cycle of PWM signal finishes. PW3C is reloaded from 0x0000 automatically, and PWM output status exchanges to high for next cycle. PW3nD decides the high duty duration, and PW3Y decides the resolution and cycle of PWM. PW3nD can't be larger than PW3Y, or the PWM signal is error. PWM clock source is Fhosc, PW3RATE[2:0] bits: 000 = Fhosc/128, 001 = Fhosc/64, 010 = Fhosc/32, 011 = Fhosc/16, 100 = Fhosc/8, 101 = Fhosc/4, 110 = Fhosc/2, 111 = Fhosc/1.



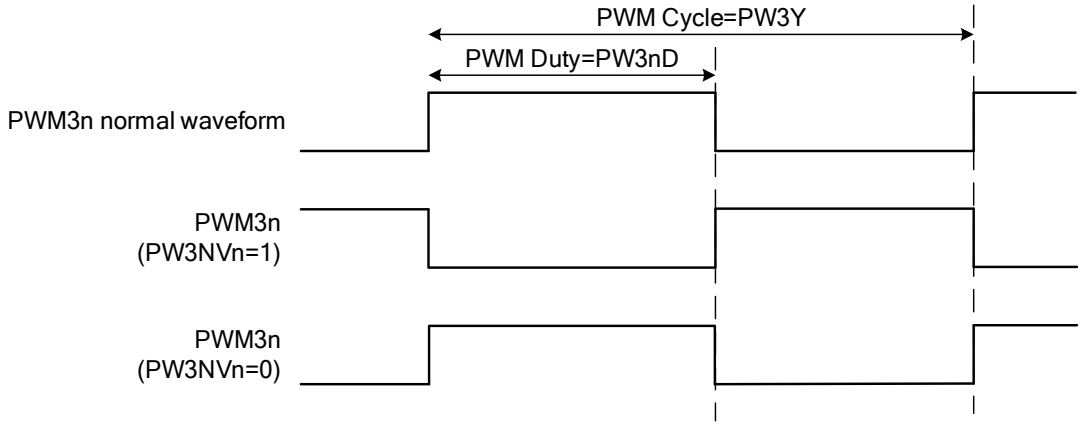
PWM Period = PW3Y

PWM duty = PW3nD/PW3Y



19.2 Inverse and Frequency Mode

The PWM builds in inverse output function. The inverse mode is controlled by PW3NV[2:0]. When PW3NVn= 1, the PWM1n outputs the inverse PWM signal of PWM. When PW3NVn = 0, the PWM3n outputs the non-inverse PWM signal of PWM. The inverse PWM output waveform is below diagram.



19.3 PWM3 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PW3M	PW3EN	PW3R2	PW3R1	PW3R0	PW3CH3	PW3CH2	PW3CH1	PW3CH0
PW3CH	-	-	-	-	PW3CH3	PW3CH2	PW3CH1	PW3CH0
PW3NV	-	-	-	-	PW3NV3	PW3NV2	PW3NV1	PW3NV0
PW3YH	PW3Y15	PW3Y14	PW3Y13	PW3Y12	PW3Y11	PW3Y10	PW3Y9	PW3Y8
PW3YL	PW3Y7	PW3Y6	PW3Y5	PW3Y4	PW3Y3	PW3Y2	PW3Y1	PW3Y0
PW30DH	PW30D15	PW30D14	PW30D13	PW30D12	PW30D11	PW30D10	PW30D9	PW30D8
PW30DL	PW30D7	PW30D6	PW30D5	PW30D4	PW30D3	PW30D2	PW30D1	PW30D0
PW31DH	PW31D15	PW31D14	PW31D13	PW31D12	PW31D11	PW31D10	PW31D9	PW31D8
PW31DL	PW31D7	PW31D6	PW31D5	PW31D4	PW31D3	PW31D2	PW31D1	PW31D0
PW32DH	PW32D15	PW32D14	PW32D13	PW32D12	PW32D11	PW32D10	PW32D9	PW32D8
PW32DL	PW32D7	PW32D6	PW32D5	PW32D4	PW32D3	PW32D2	PW32D1	PW32D0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN3	ET4	ET3	EPW4	EPW3	EPW2	EPW1	ECS	-
IRCON3	TF4	TF3	PW4F	PW3F	PW2F	PW1F	CSF	-

PW3M Register (0xF080)

Bit	Field	Type	Initial	Description
7	PW3EN	R/W	0	PW3 function 0: Disable

				1: Enable*
6..4	PW3R[2:0]	R/W	000	PWM timer clock source 000: Fhosc / 128 001: Fhosc / 64 010: Fhosc / 32 011: Fhosc / 16 100: Fhosc / 8 101: Fhosc / 4 110: Fhosc / 2 111: Fhosc / 1

* When the period is setting 0x0000, after PWM is set enable bit, the PWM will stop and the period can't update.

PW3CH Register (0xF081)

Bit	Field	Type	Initial	Description
7..3	Reserved	R/W	0000	
2	PW3CH2	R/W	0	PWM32 shared-pin control 0: GPIO 1: PWM output (shared with P1.6)
1	PW3CH1	R/W	0	PWM31 shared-pin control 0: GPIO 1: PWM output (shared with P1.5)
0	PW3CH0	R/W	0	PWM30 shared-pin control 0: GPIO 1: PWM output (shared with P1.4)

PW3NV Register (0xF082)

Bit	Field	Type	Initial	Description
7..3	Reserved	R/W	0000	
2	PW3NV2	R/W	0	PWM32 inverse output control 0: PWM32 outputs non-inverse PWM signal 1: PWM32 outputs inverse PWM signal
1	PW3NV1	R/W	0	PWM31 inverse output control 0: PWM31 outputs non-inverse PWM signal 1: PWM31 outputs inverse PWM signal
0	PW3NV0	R/W	0	PWM30 inverse output control 0: PWM30 outputs non-inverse PWM signal 1: PWM30 outputs inverse PWM signal

PW3YH/PW3YL Registers (PW3YH: 0xF086, PW3YL: 0xF087)

Bit	Field	Type	Initial	Description
7..0	PW3YH/L	R/W	0x00	16-bit PWM3 period control*.

* The period configuration must be setup completely before starting PWM function.

PW30DH/PW30DL Registers (PW30DH: 0xF0A0, PW30DL: 0xF0A1)

Bit	Field	Type	Initial	Description
7..0	PW30DH/L	R/W	0x00	16-bit PWM3 duty control.

PW31DH/PW31DL Registers (PW31DH: 0xF0A2, PW31DL: 0xF0A3)

Bit	Field	Type	Initial	Description
7..0	PW31DH/L	R/W	0x00	16-bit PWM3 duty control.

PW32DH/PW32DL Registers (PW32DH: 0xF0A4, PW32DL: 0xF0A5)

Bit	Field	Type	Initial	Description
7..0	PW32DH/L	R/W	0x00	16-bit PWM3 duty control.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN3 Register (0xEC)

Bit	Field	Type	Initial	Description
4	EPW3	R/W	0	PWM3 interrupt control bit. 0: Disable PWM3 interrupt function. 1: Enable PWM3 interrupt function.
Else				Refer to other chapter(s)

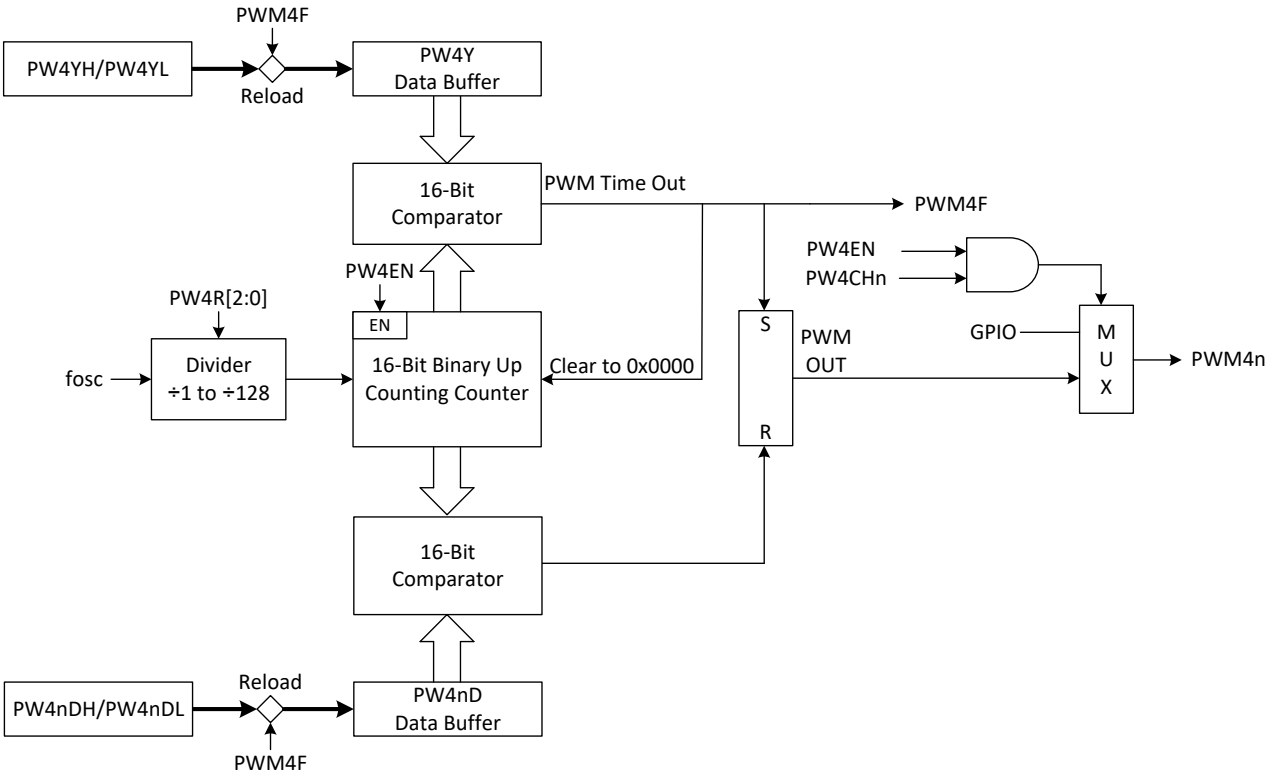
IRCON3 Register (0xED)

Bit	Field	Type	Initial	Description
4	PW3F	R/W	0	PWM3 interrupt request flag. 0: None PWM3 interrupt request 1: PWM3 interrupt request.
Else				Refer to other chapter(s)

20 PWM4

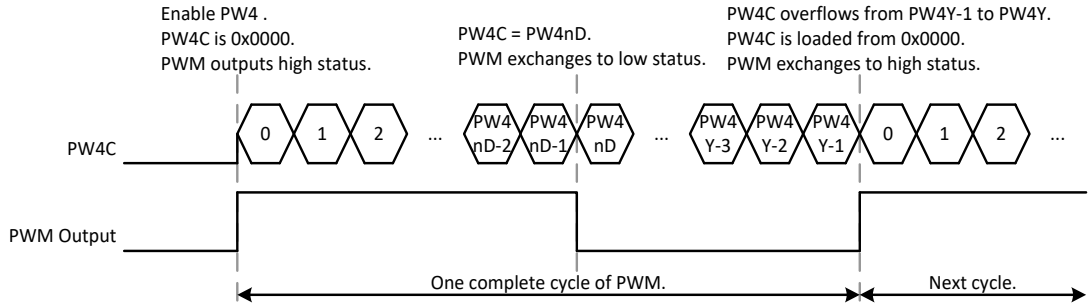
The PW4 timer is a 16-bit up counting timer and supports 4-channel general PWM function. By the counter reaches the up-boundary value PW4Y, it clears its counter and triggers an interrupt signal. PWM's duty cycle is controlled by PW40D~PW43D register. Each PWM channel has its own duty control.

The PWM function has 4 programmable channels shared with GPIO pins and controlled by PW4CH[3:0] bits. The output operation must be through enabled each bit/channel of PW4CH[3:0] bits. The enabled PWM channel exchanges from GPIO to PWM output. When the PW4CH[3:0] bits disables, the PWM channel returns to last status of GPIO mode. The PW4 timer builds in IDLE Mode wake-up function if interrupt enable. When timer overflow occurs (counts from PW4Y-1 to PW4Y), PW4F would be issued immediately which can read/write by firmware. PW4 interrupt function is controlled by EPW4.



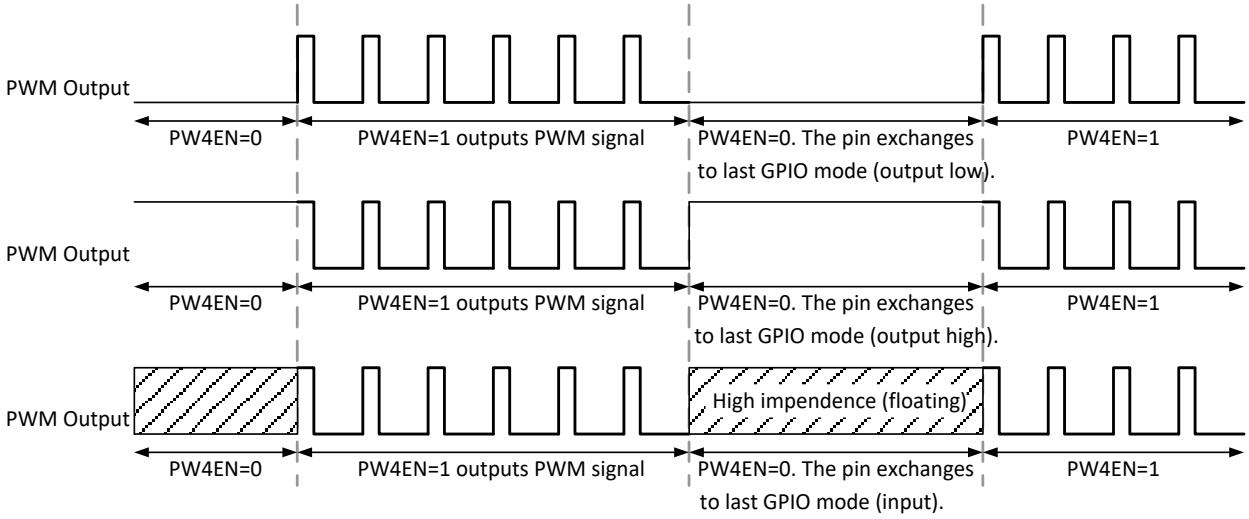
20.1 General PWM

PW4 timer builds in PWM function controlled by PW4EN register and PW4CH bits. PWM40 - PWM43 are output pins. Those output pins are shared with GPIO pin controlled by PW4CH[3:0] bits. When output PWM function, we must be set PW4EN =1. When PWM output signal synchronize finishes, the PWM channel exchanges from GPIO to PWM output. When PW4EN = 0, the PWM channel returns to GPIO mode and last status. PWM signal is generated from the result of PW4Y and PW4nD comparison combination. When PW4C starts to count or returns to 0x0000, the PWM outputs high status which is the PWM initial status. PW4C is loaded new data from PW4Y register to decide PWM cycle and resolution. PW4C keeps counting, and the system compares PW4C and PW4nD. When PW4C=PW4nD, the PWM output status exchanges to low and PW4C keeps counting. When PW4 timer overflow occurs (PW4Y-1 to 0x0000), and one cycle of PWM signal finishes. PW4C is reloaded from 0x0000 automatically, and PWM output status exchanges to high for next cycle. PW4nD decides the high duty duration, and PW4Y decides the resolution and cycle of PWM. PW4nD can't be larger than PW4Y, or the PWM signal is error. PWM clock source is Fhosc, PW4RATE[2:0] bits: 000 = Fhosc/128, 001 = Fhosc/64, 010 = Fhosc/32, 011 = Fhosc/16, 100 = Fhosc/8, 101 = Fhosc/4, 110 = Fhosc/2, 111 = Fhosc/1.



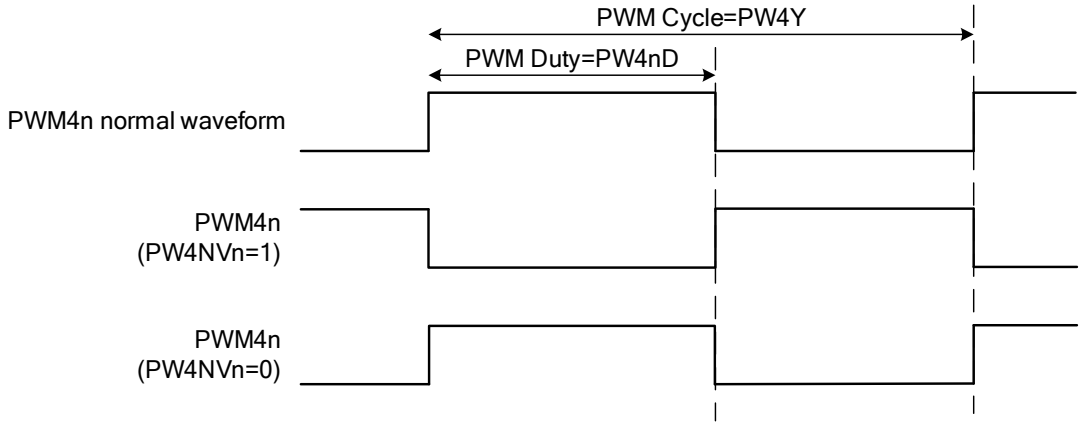
PWM Period = PW4Y

PWM duty = PW4nD/PW4Y



20.2 Inverse and Frequency Mode

The PWM builds in inverse output function. The inverse mode is controlled by PW4NV[3:0]. When PW4NVn= 1, the PWM1n outputs the inverse PWM signal of PWM. When PW4NVn = 0, the PWM4n outputs the non-inverse PWM signal of PWM. The inverse PWM output waveform is below diagram.



20.3 PWM4 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PW4M	PW4EN	PW4R2	PW4R1	PW4R0	PW4CH3	PW4CH2	PW4CH1	PW4CH0
PW4CH	-	-	-	-	PW4CH3	PW4CH2	PW4CH1	PW4CH0
PW4NV	-	-	-	-	PW4NV3	PW4NV2	PW4NV1	PW4NV0
PW4YH	PW4Y15	PW4Y14	PW4Y13	PW4Y12	PW4Y11	PW4Y10	PW4Y9	PW4Y8
PW4YL	PW4Y7	PW4Y6	PW4Y5	PW4Y4	PW4Y3	PW4Y2	PW4Y1	PW4Y0
PW40DH	PW40D15	PW40D14	PW40D13	PW40D12	PW40D11	PW40D10	PW40D9	PW40D8
PW40DL	PW40D7	PW40D6	PW40D5	PW40D4	PW40D3	PW40D2	PW40D1	PW40D0
PW41DH	PW41D15	PW41D14	PW41D13	PW41D12	PW41D11	PW41D10	PW41D9	PW41D8
PW41DL	PW41D7	PW41D6	PW41D5	PW41D4	PW41D3	PW41D2	PW41D1	PW41D0
PW42DH	PW42D15	PW42D14	PW42D13	PW42D12	PW42D11	PW42D10	PW42D9	PW42D8
PW42DL	PW42D7	PW42D6	PW42D5	PW42D4	PW42D3	PW42D2	PW42D1	PW42D0
PW43DH	PW43D15	PW43D14	PW43D13	PW43D12	PW43D11	PW43D10	PW43D9	PW43D8
PW43DL	PW43D7	PW43D6	PW43D5	PW43D4	PW43D3	PW43D2	PW43D1	PW43D0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN3	ET4	ET3	EPW4	EPW3	EPW2	EPW1	ECS	-
IRCON3	TF4	TF3	PW4F	PW3F	PW2F	PW1F	CSF	-

PW4M Register (0xF088)

Bit	Field	Type	Initial	Description

7	PW4EN	R/W	0	PW4 function 0: Disable 1: Enable*
6..4	PW4R[2:0]	R/W	000	PWM timer clock source 000: Fhosc / 128 001: Fhosc / 64 010: Fhosc / 32 011: Fhosc / 16 100: Fhosc / 8 101: Fhosc / 4 110: Fhosc / 2 111: Fhosc / 1

* When the period is setting 0x0000, after PWM is set enable bit, the PWM will stop and the period can't update.

PW4CH Register (0xF089)

Bit	Field	Type	Initial	Description
7..4	Reserved	R/W	0000	
3	PW4CH3	R/W	0	PWM43 shared-pin control 0: GPIO 1: PWM output (shared with P3.7)
2	PW4CH2	R/W	0	PWM42 shared-pin control 0: GPIO 1: PWM output (shared with P3.6)
1	PW4CH1	R/W	0	PWM41 shared-pin control 0: GPIO 1: PWM output (shared with P3.5)
0	PW4CH0	R/W	0	PWM40 shared-pin control 0: GPIO 1: PWM output (shared with P3.4)

PW4NV Register (0xF08A)

Bit	Field	Type	Initial	Description
7..4	Reserved	R/W	0000	
3	PW4NV3	R/W	0	PWM43 inverse output control 0: PWM43 outputs non-inverse PWM signal 1: PWM43 outputs inverse PWM signal
2	PW4NV2	R/W	0	PWM42 inverse output control 0: PWM42 outputs non-inverse PWM signal

				1: PWM42 outputs inverse PWM signal
1	PW4NV1	R/W	0	PWM41 inverse output control 0: PWM41 outputs non-inverse PWM signal 1: PWM41 outputs inverse PWM signal
0	PW4NV0	R/W	0	PWM40 inverse output control 0: PWM40 outputs non-inverse PWM signal 1: PWM40 outputs inverse PWM signal

PW4YH/PW4YL Registers (PW4YH: 0xF08E, PW4YL: 0xF08F)

Bit	Field	Type	Initial	Description
7..0	PW4YH/L	R/W	0x00	16-bit PWM4 period control*.

* The period configuration must be setup completely before starting PWM function.

PW40DH/PW40DL Registers (PW40DH: 0xF0A8, PW40DL: 0xF0A9)

Bit	Field	Type	Initial	Description
7..0	PW40DH/L	R/W	0x00	16-bit PWM4 duty control.

PW41DH/PW41DL Registers (PW41DH: 0xF0AA, PW41DL: 0xF0AB)

Bit	Field	Type	Initial	Description
7..0	PW41DH/L	R/W	0x00	16-bit PWM4 duty control.

PW42DH/PW42DL Registers (PW42DH: 0xF0AC, PW42DL: 0xF0AD)

Bit	Field	Type	Initial	Description
7..0	PW42DH/L	R/W	0x00	16-bit PWM4 duty control.

PW43DH/PW43DL Registers (PW43DH: 0xF0AE, PW43DL: 0xF0AF)

Bit	Field	Type	Initial	Description
7..0	PW43DH/L	R/W	0x00	16-bit PWM4 duty control.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN3 Register (0xEC)

Bit	Field	Type	Initial	Description

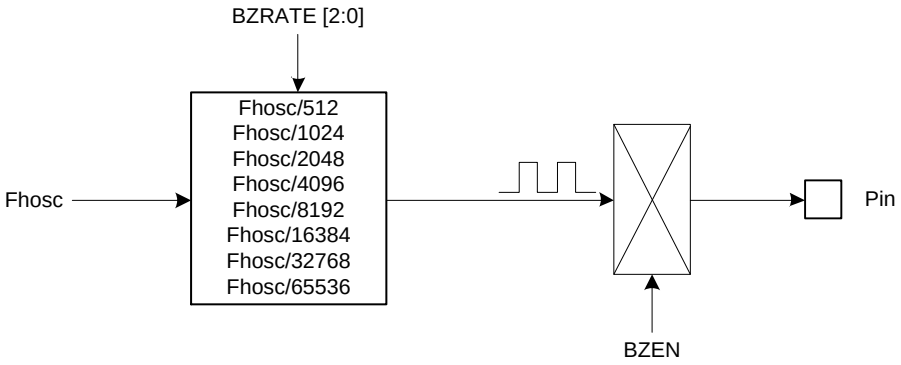
5	EPW4	R/W	0	PWM4 interrupt control bit. 0: Disable PWM4 interrupt function. 1: Enable PWM4 interrupt function.
Else				Refer to other chapter(s)

IRCON3 Register (0xED)

Bit	Field	Type	Initial	Description
4	PW4F	R/W	0	PWM4 interrupt request flag. 0: None PWM4 interrupt request 1: PWM4 interrupt request.
Else				Refer to other chapter(s)

21 2K/4K BUZZER GENERATOR

The MCU builds in Buzzer generator to drive external buzzer device. The buzzer generator purpose is to drive 2KHz or 4KHz buzzer. Adjusting buzzer output frequency is through BZM register. The buzzer output pin is shared with GPIO. When BZEN = 1, the pin outputs buzzer carry signal. When BZEN = 0, the pin returns to GPIO last condition (input mode, output high or output low status).



- The buzzer frequency is divided from Fhosc controlled by BZrate bits, and Fhosc decides the buzzer frequency. The selection table is as following.

BZrate [2:0]	Buzzer Rate Division	Buzzer Rate			
		IHRC_32MHz	X'tal = 16MHz	X'tal = 12MHz	X'tal = 4MHz
000	Fhosc/512	64KHz	32KHz	24KHz	8KHz
001	Fhosc/1024	32KHz	16KHz	12KHz	4KHz
010	Fhosc/2048	16KHz	8KHz	6KHz	2KHz
011	Fhosc/4096	8KHz	4KHz	3KHz	1KHz
100	Fhosc/8192	4KHz	2KHz	1.5KHz	500Hz
101	Fhosc/16384	2KHz	1KHz	750Hz	250Hz
110	Fhosc/32768	1KHz	500Hz	375Hz	125Hz
111	Fhosc/65536	500Hz	250Hz	188Hz	63Hz

- The buzzer target frequency is 2KHz and 4KHz. It is important to choice a good Fhosc rate to obtain the correct buzzer frequency. The above table shows 2KHz/4KHz buzzer frequency configurations.

21.1 Buzzer Register

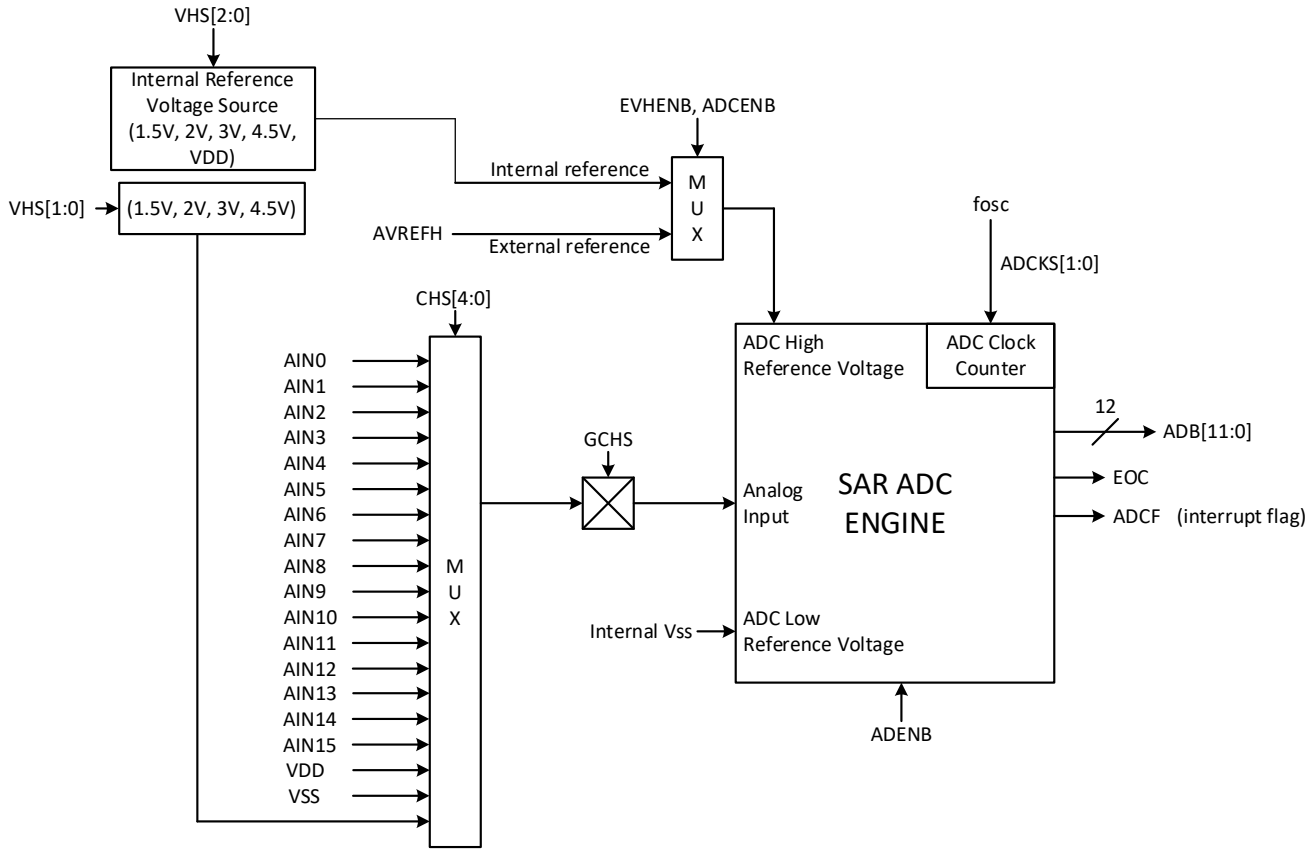
Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BZM	BZEN	BZrate2	BZrate1	BZrate0	-	-	-	-

BZM Register (0xD9)

Bit	Field	Type	Initial	Description
7	BZEN	R/W	0	Buzzer output control bit. 0: Disable BZ output and BZ output pin(P1.6) transfers to I/O last status. 1: Enable BZ output and disable GPIO(P1.6) function.
6..4	BZRATE[2:0]	R/W	000	Buzzer rate control bits. 000: Fhosc/512 001: Fhosc/1024 010: Fhosc/2048 011: Fhosc/4096 100: Fhosc/8192 101: Fhosc/16384 110: Fhosc/32768 111: Fhosc/65536
3..0	Reserved	R	0x0	

22 ADC

The analog to digital converter (ADC) is SAR structure with 16-input sources and up to 4096-step resolution to transfer analog signal into 12-bits digital buffers. The ADC builds in 16-channel input source to measure 16 different analog signal sources. The ADC resolution is 12-bit. The ADC has four clock rates to decide ADC converting rate. The ADC reference high voltage includes six sources. Five internal power source including VDD, 4.5V, 3V, 2V and 1.5V. The other one is external reference voltage input pin from AVREFH pin. The ADC builds in P4CON/P5CON registers to set pure analog input pin. After setup ADENB and ADS bits, the ADC starts to convert analog signal to digital data. ADC can work in idle mode. After ADC operating, the system would be waked up from idle mode to normal mode if interrupt enable. ADC can not work in stop mode.



22.1 Configurations of Operation

These configurations must be setup completely before starting ADC converting. ADC is configured using the following steps:

1. Choose and enable the start of conversion ADC input channel. (By CHS[4:0] bits and GCHS bit)
2. The GPIO mode of ADC input channel must be set as input mode. (By PnM register)
3. The internal pull-up resistor of ADC input channel must be disabled. (By PnUR register)
4. The configuration control bit of ADC input channel must be set. (By PnCON register)
5. Choose ADC high reference voltage. (By VREFH register)
6. Choose Clock Rate. (By ADCKS[1:0] bits)
7. After setup ADENB bits, the ADC ready to convert analog signal to digital data.

When ADC IP is enabled by ADENB bit, it is necessary to make an ADC start-up by program. Writing a 1 to the ADS bit of register ADM. After setup ADENB and ADS bits, the ADC starts to convert analog signal to digital data. The ADS bit is reset to logic 0 when the conversion is complete. When the conversion is complete, the ADC circuit will set EOC and ADCF bits to “1” and the digital data outputs in ADB and ADR registers. If ADC interrupt function is enabled (EADC = 1), the ADC interrupt request occurs and executes interrupt service routine when ADCF is “1” after ADC converting. Clear ADCF by hardware automatically in interrupt procedure.

22.2 ADC input channel

The ADC builds in 16-channel input source (AIN0 – AIN15) to measure 16 different analog signal sources controlled by CHS[4:0] and GCHS bits. The AIN18 is internal 1.5V or 2V or 3V or 4.5V input channel. There is no any input pin from outside. In this time ADC reference voltage must be internal VDD, not internal 1.5V or 2V or 3V or 4.5V. AIN18 can be a good battery detector for battery system. To select appropriate internal AVREFH level and compare value, a high performance and cheaper low battery detector is built in the system. AIN16 is VDD channel. AIN17 is VSS channel. Other channel is reserved.

CHS[4:0]	Channel	Pin name	Remark
00000	AIN0	P4.0	-
00001	AIN1	P4.1	-
00010	AIN2	P4.2	-
00011	AIN3	P4.3	-
00100	AIN4	P4.4	-
00101	AIN5	P4.5	-
00110	AIN6	P4.6	-
00111	AIN7	P4.7	-
01000	AIN8	P5.0	-
01001	AIN9	P5.1	-
01010	AIN10	P5.2	-
01011	AIN11	P5.3	-
01100	AIN12	P5.4	-
01101	AIN13	P5.5	-
01110	AIN14	P5.6	-
01111	AIN15	P5.7	-
10000	AIN16	VDD	-
10001	AIN17	VSS	-
10010	AIN18	Internal 1.5V or 2V or 3V or 4.5V	Battery detector channel
Other	-	-	Reserved

22.2.1 Pin Configuration

ADC input channels are shared with Port4 and Port5. ADC channel selection is through CHS[4:0] bit. Only one pin of Port4 and Port5 can be configured as ADC input in the same time. The pins of Port4 and Port5 configured as ADC input channel must be set input mode, disable internal pull-up and enable P4CON/P5CON first by program. After selecting ADC input channel through CHS[4:0], set GCHS bit as “1” to enable ADC channel function.

ADC input pins are shared with digital I/O pins. Connect an analog signal to CMOS digital input pin, especially, the analog signal level is about 1/2 VDD will cause extra current leakage. In the power down mode, the above leakage current will be a big problem. Unfortunately, if users connect more than one analog input signal to Port4, Port5 will encounter above current leakage situation. Write “1” into PnCON register will configure related pin as pure analog input pin to avoid current leakage.

Note that When ADC pin is general I/O mode, the bit of P4CON and P5CON must be set to “0”, or the digital I/O signal would be isolated.

22.3 Reference Voltage

The ADC builds in six high reference voltage source controlled through VREFH register. There are one external voltage source and five internal voltage source (VDD, 4.5V, 3V, 2V, 1.5V). When EVHENB bit is “1”, ADC reference voltage is external voltage source from AVREFH/P4.0. In the condition, P4.0 GPIO mode must be set as input mode and disable internal pull-up resistor.

If EVHENB bit is “0”, ADC high reference voltage is from internal voltage source selected by VHS[2:0] bits. If VHS[2:0] is “1xx”, ADC high reference voltage is VDD. If VHS[1:0] is “010”, ADC high reference voltage is 4.5V. If VHS[2:0] is “001”, ADC high reference voltage is 3V. If VHS[2:0] is “000”, ADC high reference voltage is 2V. If VHS[2:0] is “011”, ADC high reference voltage is 1.5V. The limitation of internal high reference voltage application is VDD can’t below each of internal high voltage level, or the level is equal to VDD. If AIN18 channel is selected as internal 1.5 or 2V or 3V or 4.5V input channel. There is no any input pin from outside. In this time ADC high reference voltage must be internal VDD, not internal 1.5V/2V/3V/4.5V.

22.3.1 Signal Format

ADC sampling voltage range is limited by high/low reference voltage. The ADC low reference voltage is VSS. The ADC high reference voltage includes internal VDD/4.5V/3V/2V/1.5V and external reference voltage source from P4.0/AVREFH pin controlled by EVHENB bit. ADC reference voltage range limitation is “(ADC high reference voltage - low reference voltage) ≥ 1.5V”. ADC low reference voltage is VSS = 0V. So ADC high reference voltage range is 1.5V to VDD. The range is ADC external high reference voltage range.

- ADC Internal Low Reference Voltage = 0V.
- ADC Internal High Reference Voltage = VDD/4.5V/3V/2V/1.5V. (EVHENB=0)
- ADC External High Reference Voltage = 1.5V to VDD. (EVHENB=1)

ADC sampled input signal voltage must be from ADC low reference voltage to ADC high reference. If the ADC input signal voltage is over the range, the ADC converting result is error (full scale or zero).

- ADC Low Reference Voltage ≤ ADC Sampled Input Voltage ≤ ADC High Reference Voltage

22.4 Converting Time

The ADC converting time is from ADS=1 (Start to ADC convert) to EOC=1 (End of ADC convert). The converting time duration is depend on ADC clock rate. 12-bit ADC’s converting time is
1/ (ADC clock)*16 sec. ADC only one clock sources: Fhosc, ADCKS[2:0] bits: 000 = Reserved, 001 = Fhosc/2, 010 = Fhosc/4, 011 = Fhosc/8, 100 = Fhosc/16, 101 = Fhosc/32, 110 = Fhosc/64, 111 = Fhosc/128.

The ADC converting time affects ADC performance. If input high rate analog signal, it is necessary to select a high ADC converting rate. If the ADC converting time is slower than analog signal variation rate, the ADC result would be error. So to select a correct ADC clock rate to decide a right ADC converting rate is very important.

$$12 \text{ bits ADC conversion time} = \frac{16}{\text{ADC clock rate}}$$

ADCKS[2:0]	ADC clock rate	Fhosc = 16MHz		Fhosc = 32MHz	
		Converting time	Converting rate	Converting time	Converting rate
000	Reserved	-	-	-	-
001	Fhosc/2	1/(16MHz/2)*16 = 2us	500 kHz	1/(32MHz/2)*16 = 1us	1000 kHz
010	Fhosc/4	1/(16MHz/4)*16 = 4us	250 kHz	1/(32MHz/4)*16 = 2us	500 kHz
011	Fhosc/8	1/(16MHz/8)*16 = 8us	125 kHz	1/(32MHz/8)*16 = 4us	250 kHz
100	Fhosc/16	1/(16MHz/16)*16 = 16us	62.5 kHz	1/(32MHz/16)*16 = 8us	125 kHz
101	Fhosc/32	1/(16MHz/32)*16 = 32us	31.25 kHz	1/(32MHz/32)*16 = 16us	62.5 kHz
110	Fhosc/64	1/(16MHz/64)*16 = 64us	15.625 kHz	1/(32MHz/64)*16 = 32us	31.25 kHz
111	Fhosc/128	1/(16MHz/128)*16 = 128us	7.8125 kHz	1/(32MHz/128)*16 = 64us	15.625 kHz

22.5 Data Buffer

ADC data buffer is 12-bit length to store ADC converter result. The high byte is ADB register, and the low-nibble is ADR[3:0] bits. The ADB register is only 8-bit register including bit 4 – bit 11 ADC data. To combine ADB register and the low-nibble of ADR will get full 12-bit ADC data buffer. The ADC data buffer is a read-only register and the initial status is unknown after system reset.

Table 22-1 The AIN input voltage vs. ADB output data

AIN n	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
0/4096*VREFH	0	0	0	0	0	0	0	0	0	0	0	0
1/4096*VREFH	0	0	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
4094/4096*VREFH	1	1	1	1	1	1	1	1	1	1	1	0
4095/4096*VREFH	1	1	1	1	1	1	1	1	1	1	1	1

22.6 ADC Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADM	ADENB	ADS	EOC	CHS4	CHS3	CHS2	CHS1	CHS0
ADB	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4
ADR	-	GCHS	-	-	ADB3	ADB2	ADB1	ADB0
VREFH	EVHENB	-	-	-	VREFSW	VHS2	VHS1	VHS0
ADCAL	-	-	-	-	-	ADCKS2	ADCKS1	ADCKS0
P4CON	P4CON7	P4CON6	P4CON5	P4CON4	P4CON3	P4CON2	P4CON1	P4CON0
P5CON	P5CON7	P5CON6	P5CON5	P5CON4	P5CON3	P5CON2	P5CON1	P5CON0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN2	EU3RX	EU3TX	-	-	-	ET2	EADC	ELVD
IRCON2	-	-	-	-	-	TF2	ADCF	LVDF

ADM Register (0xD2)

Bit	Field	Type	Initial	Description
7	ADENB	R/W	0	ADC control bit. In stop mode, disable ADC to reduce power consumption. 0: Disable 1: Enable
6	ADS	R/W	0	ADC conversion control. Write 1: Start ADC conversion (automatically cleared by the end of conversion)
5	EOC	R	0	ADC status bit. 0: ADC progressing 1: End of conversion
4..0	CHS[4:0]	R/W	0x00	ADC input channel select bit. 00000: AIN0, 00001: AIN1, 00010: AIN2, 00011: AIN3, 00100: AIN4, 00101: AIN5, 00110: AIN6, 00111: AIN7, 01000: AIN8, 01001: AIN9, 01010: AIN10, 01011:AIN11, 01100: AIN12, 01101: AIN13, 01110: AIN14, 01111: AIN15, 10000: VDD, 10001: VSS, 10010: AIN18*(1), Others: Reserved.

*(1) The AIN18 is internal 1.5V or 2V or 3V or 4.5V input channel. There is no any input pin from outside. In this time ADC reference voltage must be internal VDD, not internal 1.5V or 2V or 3V or 4.5V.

ADB Register (0xD3)

Bit	Field	Type	Initial	Description
7..0	ADB[11:4]	R	-	ADC Result Bit [11:4]* in 12-bit ADC resolution mode.

* ADC data buffer is 12-bit length to store ADC converter result. The high byte is ADB register, and the low-nibble is ADR[3:0] bits.

ADR Register (0xD4)

Bit	Field	Type	Initial	Description
7	Reserve	R	0	
6	GCHS	R/W	0	ADC global channel select bit. 0: Disable AIN channel 1: Enable AIN channel
5..4	Reserve	R	0	
3..0	ADB[3:0]	R	-	ADC Result Bit [3:0]* in 12-bit ADC resolution mode.

* ADC data buffer is 12-bit length to store ADC converter result. The high byte is ADB register, and the low-nibble is ADR[3:0] bits.

VREFH Register (0xD5)

Bit	Field	Type	Initial	Description
7	EVHENB	R/W	1	ADC internal reference high voltage control bit. 0: Enable ADC internal VREFH function. AVREFH/P4.0 pin is GPIO. 1: Disable ADC internal VREFH function. AVREFH/P4.0 pin is external AVREFH*(1) input pin.
6..4	Reserved	R	0	
3	VREFSW	R/W	0	High resolution internal reference voltage ADC switch control bit. 0: AVREFH pin disconnect to Internal reference output by internal switch(OFF). 1: AVREFH pin connect to Internal reference output by internal switch(ON), and connect capacitor to improve resolution.
2..0	VHS[2:0]	R/W	000	ADC internal reference high voltage selects bits. *(2) 000: VREFH = 2.0V 001: VREFH = 3.0V 010: VREFH = 4.5V 011: VREFH = 1.5V 100: VREFH = VDD and AIN18 = 2.0V 101: VREFH = VDD and AIN18 = 3.0V 110: VREFH = VDD and AIN18 = 4.5V 111: VREFH = VDD and AIN18 = 1.5V

*(1) The AVREFH level must be between the VDD and 1.5V.

*(2) If AIN18 channel is selected as internal 1.5V or 2V or 3V or 4.5V input channel. There is no any input pin from outside. In this time ADC reference high voltage must be internal VDD, not internal 1.5V/2V/3V/ 4.5V.

ADCAL Register (0xD1)

Bit	Field	Type	Initial	Description
7..3	Reserve	R	0	
2..0	ADCKS[2:0]	R/W	0	ADC's clock source select bit. 000 = Reserved, 001 = Fhosc/2, 010 = Fhosc/4, 011 = Fhosc/8, 100 = Fhosc/16, 101 = Fhosc/32, 110 = Fhosc/64, 111 = Fhosc/128

P4CON Register (0xF014)

Bit	Field	Type	Initial	Description
7..0	P4CON[7:0]	R/W	0x00	P4 configuration control bit*. 0: P4 can be analog input pin (ADC input pin) or digital GPIO pin. 1: P4 is pure analog input pin and can't be a digital GPIO pin.

* P4CON [7:0] will configure related Port4 pin as pure analog input pin to avoid current leakage.

P5CON Register (0xF015)

Bit	Field	Type	Initial	Description
7..0	P5CON[7:0]	R/W	0x00	P5 configuration control bit*. 0: P5 can be analog input pin (ADC input pin) or digital GPIO pin. 1: P5 is pure analog input pin and can't be a digital GPIO pin.

* P5CON [7:0] will configure related Port5 pin as pure analog input pin to avoid current leakage.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN2 Register (0xC8)

Bit	Field	Type	Initial	Description
1	EADC	R/W	0	ADC interrupt control bit. 0: Disable ADC interrupt function. 1: Enable ADC interrupt function.
Else				Refer to other chapter(s)

IRCON2 Register (0xA7)

Bit	Field	Type	Initial	Description
1	ADCF	R/W	0	ADC interrupt request flag. 0 = None ADC interrupt request. 1 = ADC interrupt request.
Else				Refer to other chapter(s)

23 UART0/1/2/3

The UARTn (n=0,1,2,3 in the following descriptions) provides a flexible full-duplex synchronous/asynchronous receiver/transmitter. The serial interface provides an up to 500 kHz flexible full-duplex transmission. It can operate in four modes (one synchronous and three asynchronous). Mode 0 is a shift register mode and operates as synchronous transmitter/receiver. In Mode 1-Mode 3 the UART operates as asynchronous transmitter/receiver with 8-bit or 9-bit data. The transfer format has start bit, 8-bit/ 9-bit data and stop bit. Transmission is started by writing to the SnBUF register. After reception, input data are available after completion of the reception in the SnBUF register. TB8n/RB8n bit can be used as the 9th bit for transmission and reception in 9-bit UART mode. Programmable baud rate supports different speed peripheral devices.

The UART features include the following:

- Full-duplex, 2-wire synchronous/asynchronous data transfer.
- Programmable baud rate.
- 8-bit shift register: operates as synchronous transmitter/receiver
- 8-bit / 9-bit UART: operates as asynchronous transmitter/receiver with 8 or 9-bit data bits and programmable baud rate.

23.1 UART Operation

The UARTn UTXn and URXn pins are shared with GPIO. In synchronous mode, the UTXn/URXn shared pins must set output high by software. In asynchronous mode (8-bit/9-bit UART), the UTXn shared pins must set output high and URXn set input high by software. Thus, URXn/UTXn pins will transfers to UART purpose. When UART disables, the UART pins returns to GPIO last status.

The UTXn/URXn pins also support open-drain structure. The open-drain option is controlled by PnOC bit. When PnOC=0, disable UTXn/URXn open-drain structure. When PnOC=1, enable UTXn/URXn open-drain structure. If enable open-drain structure, UTXn/URXn pin must set high level (IO mode control will be ignored) and need external pull-up resistor.

The UARTn supports interrupt function. EUnTX and EUnRX are UARTn transfer interrupt function control bits. UARTn transmitter and receiver interrupt function is controlled by EUnTX and EUnRX respectively. EUnTX=0/EUnRX=0, disable transmitter/receiver interrupt function. EUnTX=1/ EUnRX=1, enable UART transmitter/receiver interrupt function. When UARTn interrupt function enables, the program counter points to interrupt vector to do UARTn interrupt service routine after UART operating. TIn/RIn is UARTn interrupt request flag, and also to be the UART operating status indicator when interrupt is disabled. TIn and RIn must clear by software.

UARTn provides four operating mode (one synchronous and three asynchronous) controlled by SnCON register. These modes can be support in different baud rate and communication protocols.

S0M0	S0M1	Mode	Synchronization	Clock Rate	Start Bit	Data Bits	Stop Bit	UART pins' mode and data
0	0	0	Synchronous	Fcpu/12	X	8	X	**UTX0 pin:** P02M=1 and P02=1 **URX0 pin:** Transmitter: P03M=1 and P03=1 Receiver: P03M=0 and P03=1 **UTX1 pin:** P05M=1 and P05=1 P07M=1 and P07=1 **URX1 pin:** Transmitter: P06M=1 and P06=1 P07M=1 and P07=1 Receiver: P06M=0 and P06=1 P07M=0 and P07=1 **UTX2 pin:** P13M=1 and P13=1 **URX2 pin:** Transmitter: P14M=1 and P14=1 Receiver: P14M=0 and P14=1 **UTX3 pin:** P13M=1 and P13=1 **URX3 pin:** Transmitter: P61M=1 and P61=1 Receiver: P62M=0 and P62=1
0	1	1	Asynchronous	Baud rate generator or T1 overflow rate	1	8	1	UTX/URX pin mode and data switch by

1	0	2	Asynchronous	Fcpu/64 or Fcpu/32	1	9	1	hardware.
1	1	3	Asynchronous	Baud rate generator or T1 overflow rate	1	9	1	

23.2 Mode 0: Synchronous 8-bit Receiver/Transmitter

Mode 0 is a shift register mode. It operates as synchronous transmitter/receiver. The UTXn pin output shift clock for both transmit and receive condition. The URXn pin is used to transmit and receive data. 8-bit data will be transmit and receive with LSB first. The baud rate is Fcpu/12. Data transmission is started by writing data to SnBUF register. In the end of the 8th bit transmission, the TIn flag is set. Data reception is controlled by RENn bit and clearing RIn bits. When RENn=1 and RIn is from 1 to 0, data transmission starts and the RIn flag is set at the end of the 8th bit reception.

✷ ***Note:***

1. Only Mode 0, the URXn and UTXn respectively require input and output mode selection to receive/transmit data appropriately.

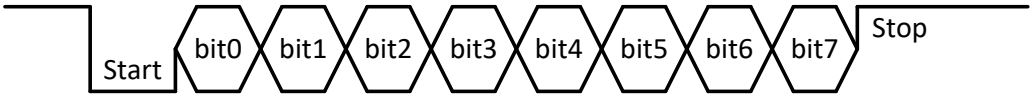
2. Setting P02 and P03 initially high because UART block drive the shared pin low signal only.

23.3 Mode 1: 8-bit Receiver/Transmitter with Variable Baud Rate

Mode 1 supports an asynchronous 8-bit UART with variable baud rate. The transfer format includes 1 start bit, 8 data bits (LSB first) and 1 stop bit. Data is transmitted by UTXn pin and received by URXn pin. The baud rate clock source can be baud rate generator or T1 overflow controlled by BDn bit. When BDn=0, the baud rate clock source is from T1 overflow. When BDn=1, the baud rate clock source is from baud rate generator controlled by SnRELH and SnRELL. Additionally, the baud rate can be doubled by SMODn bit.

Data transmission is controlled by TENn bit. After transmission configuration, load transmitted data into SnBUF, and then UARTn starts to transmit the pocket. The TIn flag is set at the beginning of the stop bit.

Data reception is controlled by RENn bit. When RENn=1, data reception function is enabled. Data reception starts by receiving the start bit for master terminal, URXn detects the falling edge of start bit, and then the RIn flag is set in the middle of a stop bit. Until reception completion, input data is stored in SnBUF register and the stop bit is stored in RB8n.



23.4 Mode 2: 9-bit Receiver/Transmitter with Fixed Baud Rate

Mode 2 supports an asynchronous 9-bit UART with fixed baud rate. The transfer format includes 1 start bit, 9 data bits (LSB first) and 1 stop bit. Data is transmitted by UTXn pin and received by URXn pin. The baud rate clock source is fixed to Fcpu/64 or Fcpu/32 and is controlled by SMODn bit. When SMODn=0, baud rate is Fcpu/64. When SMODn=1, baud rate is Fcpu/32.

Data transmission is controlled by TENn bit. After transmission configuration, load transmitted data into SnBUF, and then UARTn starts to transmit the pocket. The 9th data bit is taken from TB8n. The TIn flag is set at the beginning of the stop bit.

Data reception is controlled by RENn bit. When RENn=1, data reception function is enabled. Data reception starts by receiving the start bit for master terminal, URXn detects the falling edge of start bit, and then the RIn flag is set in the middle of a stop bit. Until reception completion, lower 8-bit input data is stored in SnBUF register and the 9th bit is stored in RB8n.

23.5 Mode 3: 9-bit Receiver/Transmitter with Variable Baud Rate

Mode 3 supports an asynchronous 9-bit UART with variable baud rate. The transfer format includes 1 start bit, 9 data bits (LSB first) and 1 stop bit. Data is transmitted by UTXn pin and received by URXn pin. The different between Mode 2 and Mode 3 is baud rate selection. In the Mode 3, the baud rate clock source can be baud rate generator or T1 overflow controlled by BDn bit. When BDn=0, the baud rate clock source is from T1 overflow. When BDn=1, the baud rate clock source is from baud rate generator controlled by SnRELH and SnRELL. Additionally, the baud rate can be doubled by SMODn bit.

Data transmission is controlled by TENn bit. After transmission configuration, load transmitted data into SnBUF, and then UART starts to transmit the pocket. The 9th data bit is taken from TB8n. The TIn flag is set at the beginning of the stop bit.

Data reception is controlled by RENn bit. When RENn=1, data reception function is enabled. Data

reception starts by receiving the start bit for master terminal, URXn detects the falling edge of start bit, and then the RIn flag is set in the middle of a stop bit. Until reception completion, lower 8-bit input data is stored in SnBUF register and the 9th bit is stored in RB8n.

23.6 Multiprocessor Communication

UART supports multiprocessor communication between a master device and one or more slave device in Mode 2 and Mode 3 (9-bit UART). The master identifies correct slaves by using the 9th data bit. When the communication starts, the master transmits a specific address byte with the 9th bit is set “1” to selected slaves, and then transmits a data byte with the 9th bit is set “0” in the following transmission.

Multiprocessor communication is controlled by SnM20 bit. When SnM20=0, disable multiprocessor communication. When SnM20=1, enable multiprocessor communication. If SnM20 is set, the UARTn reception interrupt is only generated when the 9th received bit is “1” (RB8n). The slaves will compare received data with its own address data by software. If address byte is match, the slaves clear SnM20 bit to enable interrupt function in the following data transmission. The slaves with unmatched address, their SnM20 keep in “1” and will not generate interrupt in the following data transmission.

23.7 Baud Rate Control

The UARTn mode 0 has a fixed baud rate at Fcpu/12, and the mode 2 has two baud rate selection which is chosen by SMODn bit: Fcpu/64 (SMODn = 0) and Fcpu/32 (SMODn = 1).

The baud rate of UARTn mode 1 and mode 3 is generated by either SnRELH/SnRELL registers (BDn = 1) or Timer 1 overflow period (BDn = 0). The SMODn bit doubles the frequency from the generator.

If the SnRELH/SnRELL is selected (BDn = 1) in mode 1 and 3, the baud rate is generated as following equation.

$$\text{Baud Rate} = 2^{\text{SMODn}} \times \frac{\text{Fcpu}}{(64 - 8 \times \text{CDn}) \times (1024 - \text{SnREL})} bps$$

Table 23-1 Recommended Setting for Common UARTn Baud Rates (Fcpu = 16 MHz, CDn=0)

Baud Rate	SMODn	CDn	SnRELH	SnRELL	Accuracy
4800	0	0	0x03	0xCC	0.16 %
9600	0	0	0x03	0xE6	0.16 %
19200	0	0	0x03	0xF3	0.16 %
38400	1	0	0x03	0xF3	0.16 %
56000	1	0	0x03	0xF7	-0.79 %
57600	1	1	0x03	0xF6	-0.79 %
115200	1	1	0x03	0xFB	-0.79 %
128000	1	0	0x03	0xFC	-2.34 %
250000	1	0	0x03	0xFE	0.00 %
500000	1	0	0x03	0xFF	0.00 %

If the Timer 1 overflow period is selected (BDn = 0) in mode 1 and 3, the baud rate is generated as following equation. The Timer 1 must be in 8-bit auto-reload mode which can generate periodically overflow signals.

$$\text{Baud Rate} = 2^{\text{SMODn}} \times \frac{1}{(32 - 4 \times \text{CDn}) \times \text{Timer1 period}}\ bps$$

Table 23-2 Recommended Setting T1 overflow period (T1 clock=32M) for Common UART0 Baud Rates (Fcpu = 16 MHz)

Baud Rate	SMODn	CDn	Timer Period	TH1/TL1	Accuracy
4800	0	0	6.510 us	0x30	0.16 %
9600	1	0	6.510 us	0x30	0.16 %
19200	1	0	3.255 us	0x98	0.16 %
38400	1	0	1.628 us	0xCC	0.16 %
56000	1	0	1.116 us	0xDC	-0.79 %
57600	1	0	1.085 us	0xDD	-0.79 %
115200	1	1	0.543 us	0xEC	-0.79 %
128000	1	1	0.488 us	0xEE	-0.79 %
250000	1	0	0.250 us	0xF8	0.00 %

✷ ***Note:***

1. When baud rate generator source is T1 overflow rate, the max counter value is 0xFB. (Only supports 0x00~0xFB).

2. When baud rate generator source is T1 overflow rate, the system clock fcpu must

be greater four times to T1 overflow rate.

23.8 Power Saving

The UARTn module has clock gating function for saving power. When RENn bit is 0, the UARTn module internal clocks are halted to reduce power consumption. Conversely, when RENn bit is 1, UARTn internal clocks are run, and registers can access.

23.9 UART0 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SMODCAL	SMOD3	SMOD2	SMOD1	SMOD0	CD3	CD2	CD1	CD0
S0CON2	BD3	BD2	BD1	BD0	TEN3	TEN2	TEN1	TEN0
S0CON	S0M0	S0M1	S0M20	REN0	TB80	RB80	TI0	RI0
S0BUF	S0BUF7	S0BUF6	S0BUF5	S0BUF4	S0BUF3	S0BUF2	S0BUF1	S0BUF0
S0RELH	-	-	-	-	-	-	S0REL9	S0REL8
S0RELL	S0REL7	S0REL6	S0REL5	S0REL4	S0REL3	S0REL2	S0REL1	S0REL0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN1	EU2RX	EU2TX	EU1RX	EU1TX	EU0RX	EU0TX	-	EI2C
ODCON	-	-	-	SPI0OD	URT3OD	URT2OD	URT1OD	URT0OD

SMODCAL Register (0x95)

Bit	Field	Type	Initial	Description
4	SMOD0	R/W	0	UART0 baud rate control In UART mode 0: Unused. In UART mode 1, 3: The baud rate generated as the equation in section 23.7 (Baud Rate Control). In UART mode 2: 0: Fcpu/64 1: Fcpu/32
0	CD0	R/W	0	UART0 clock divider 0: 16-clocks for a cycle 1: 14-clocks for a cycle
Else				Refer to other chapter(s)

S0CON2 Register (0x96)

Bit	Field	Type	Initial	Description
4	BD0	R/W	0	UART0 Baud rate generators selection (mode 1, 3) 0: Timer 1 overflow period 1: Controlled by S0RELH and S0RELL registers
0	TEN0	R/W	0	UART0 TX enable bit 0: Disable 1: Enable
Else				Refer to other chapter(s)

S0CON Register (0x97)

Bit	Field	Type	Initial	Description
7..6	S0M[1:0]	R/W	00	UART0 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	S0M20	R/W	0	Multiprocessor communication (mode 2, 3) 0: Disable 1: Enable
4	REN0	R/W	0	UART0 module (and reception function) 0: Disable for power saving* 1: Enable for UART operating
3	TB80	R/W	0	The 9th bit transmission data (mode 2, 3)
2	RB80	R/W	0	The 9th bit data from reception
1	TI0	R/W	0	UART0 interrupt flag of transmission
0	RI0	R/W	0	UART0 interrupt flag of reception

✷ ***Note: TI0 and RI0 are clear by software when interrupt is enabled.***

S0BUF Register (0x99)

Bit	Field	Type	Initial	Description
7..0	S0BUF[7:0]	R/W	0x00	Action of writing data triggers UART0 communication (LSB first). Reception data is available to read by the end of packages.

S0RELH/S0RELL Registers (S0RELH: 0x9B, S0RELL: 0x9A)

Bit	Field	Type	Initial	Description
15..10	Reserved	R	0x00	
9..0	S0REL[9:0]	R/W	0x3D9	S0RELH[1:0] & S0RELL[7:0]. UART0 Reload Register used for UART0 baud rate generation.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN1 Register (0xB8)

Bit	Field	Type	Initial	Description
3	EU0RX	R/W	0	UART0 receiver interrupt enable
2	EU0TX	R/W	0	UART0 transmitter interrupt enable
Else				Refer to other chapter(s)

ODCON Register (0xF018)

Bit	Field	Type	Initial	Description
0	UART0OD	R/W	0	UART0 TX/RX open-drain control bit. 0: Disable, Switch UTX0 and URX0 to push-pull mode 1: Enable, Switch UTX0 and URX0 to open-drain mode
Else				Refer to other chapter(s)

23.10 UART1 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SMODMX	-	-	-	-	UR1MX1	UR1MX0	-	-
SMODCAL	SMOD3	SMOD2	SMOD1	SMOD0	CD3	CD2	CD1	CD0
S0CON2	BD3	BD2	BD1	BD0	TEN3	TEN2	TEN1	TEN0
S1CON	S1M0	S1M1	S1M20	REN1	TB81	RB81	TI1	RI1
S1BUF	S1BUF7	S1BUF6	S1BUF5	S1BUF4	S1BUF3	S1BUF2	S1BUF1	S1BUF0
S1RELH	-	-	-	-	-	-	S1REL9	S1REL8
S1RELL	S1REL7	S1REL6	S1REL5	S1REL4	S1REL3	S1REL2	S1REL1	S1REL0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN1	EU2RX	EU2TX	EU1RX	EU1TX	EU0RX	EU0TX	-	EI2C
ODCON	-	-	-	SPI0OD	URT3OD	URT2OD	URT1OD	URT0OD

SMODMX Register (0x94)

Bit	Field	Type	Initial	Description
3..2	UR1MX[1:0]	R/W	00	UART1 IO select 00: UTX1 is P05 and URX1 is P06 01: Reserved 10: UTX1(1) is P07 11: URX1(1) is P07
Else				Refer to other chapter(s)

SMODCAL Register (0x95)

Bit	Field	Type	Initial	Description
5	SMOD1	R/W	0	UART1 baud rate control. In UART mode 0: Unused. In UART mode 1, 3: The baud rate generated as the equation in section 23.7 (Baud Rate Control). In UART mode 2: 0: Fcpu/64 1: Fcpu/32
1	CD1	R/W	0	UART1 clock divider 0: 16-clocks for a cycle 1: 14-clocks for a cycle
Else				Refer to other chapter(s)

S0CON2 Register (0x96)

Bit	Field	Type	Initial	Description
5	BD1	R/W	0	UART1 Baud rate generators selection (mode 1, 3) 0: Timer 1 overflow period 1: Controlled by S1RELH and S1RELL registers
1	TEN1	R/W	0	UART1 TX enable bit 0: Disable 1: Enable
Else				Refer to other chapter(s)

S1CON Register (0xC1)

Bit	Field	Type	Initial	Description
7..6	S1M[0:1]	R/W	00	UART1 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	S1M20	R/W	0	Multiprocessor communication (mode 2, 3) 0: Disable 1: Enable
4	REN1	R/W	0	UART1 module (and reception function) 0: Disable for power saving* 1: Enable for UART operating
3	TB81	R/W	0	The 9th bit transmission data (mode 2, 3)

2	RB81	R/W	0	The 9th bit data from reception
1	TI1	R/W	0	UART1 interrupt flag of transmission
0	RI1	R/W	0	UART1 interrupt flag of reception

✷ ***Note: TI1 and RI1 are clear by software when interrupt is enabled.***

S1BUF Register (0x9D)

Bit	Field	Type	Initial	Description
7..0	S1BUF[7:0]	R/W	0x00	Action of writing data triggers UART1 communication (LSB first). Reception data is available to read by the end of packages.

S1RELH/SRRELL Registers (S1RELH: 0x9F, S1RELL: 0x9E)

Bit	Field	Type	Initial	Description
15..10	Reserved	R	0x0	
9..0	S1REL[9:0]	R/W	0x3D9	S1RELH[1:0] & S1RELL[7:0]. UART1 Reload Register used for UART1 baud rate generation.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN1 Register (0xB8)

Bit	Field	Type	Initial	Description
5	EU1RX	R/W	0	UART1 receiver interrupt enable
4	EU1TX	R/W	0	UART1 transmitter interrupt enable
Else				Refer to other chapter(s)

ODCON Register (0xF018)

Bit	Field	Type	Initial	Description
1	UART1OD	R/W	0	UART1 TX/RX open-drain control bit. 0: Disable, Switch UTX1 and URX1 to push-pull mode 1: Enable, Switch UTX1 and URX1 to open-drain mode
Else				Refer to other chapter(s)

23.11 UART2 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SMODCAL	SMOD3	SMOD2	SMOD1	SMOD0	CD3	CD2	CD1	CD0
S0CON2	BD3	BD2	BD1	BD0	TEN3	TEN2	TEN1	TEN0
S2CON	S2M0	S2M1	S2M20	REN2	TB82	RB82	TI2	RI2
S2BUF	S2BUF7	S2BUF6	S2BUF5	S2BUF4	S2BUF3	S2BUF2	S2BUF1	S2BUF0
S2RELH	-	-	-	-	-	-	S2REL9	S2REL8
S2RELL	S2REL7	S2REL6	S2REL5	S2REL4	S2REL3	S2REL2	S2REL1	S2REL0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN1	EU2RX	EU2TX	EU1RX	EU1TX	EU0RX	EU0TX	-	EI2C
ODCON	-	-	-	SPI0OD	URT3OD	URT2OD	URT1OD	URT0OD

SMODCAL Register (0x95)

Bit	Field	Type	Initial	Description
6	SMOD2	R/W	0	UART2 baud rate control. In UART mode 0: Unused. In UART mode 1, 3: The baud rate generated as the equation in section 23.7 (Baud Rate Control). In UART mode 2: 0: Fcpu/64 1: Fcpu/32
2	CD2	R/W	0	UART2 clock divider 0: 16-clocks for a cycle 1: 14-clocks for a cycle
Else				Refer to other chapter(s)

S0CON2 Register (0x96)

Bit	Field	Type	Initial	Description
6	BD2	R/W	0	UART2 Baud rate generators selection (mode 1, 3) 0: Timer 1 overflow period 1: Controlled by S2RELH and S2RELL registers
2	TEN2	R/W	0	UART2 TX enable bit 0: Disable 1: Enable

Else	Refer to other chapter(s)

S2CON Register (0xA1)

Bit	Field	Type	Initial	Description
7..6	S2M[0:1]	R/W	00	UART2 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	S2M20	R/W	0	Multiprocessor communication (mode 2, 3) 0: Disable 1: Enable
4	REN2	R/W	0	UART2 module (and reception function) 0: Disable for power saving* 1: Enable for UART operating
3	TB82	R/W	0	The 9th bit transmission data (mode 2, 3)
2	RB82	R/W	0	The 9th bit data from reception
1	TI2	R/W	0	UART2 interrupt flag of transmission
0	RI2	R/W	0	UART2 interrupt flag of reception

✷ ***Note: TI2 and RI2 are clear by software when interrupt is enabled.***

S2BUF Register (0xA2)

Bit	Field	Type	Initial	Description
7..0	S2BUF[7:0]	R/W	0x00	Action of writing data triggers UART2 communication (LSB first). Reception data is available to read by the end of packages.

S2RELH/S2RELL Registers (S2RELH: 0xA4, S2RELL: 0xA3)

Bit	Field	Type	Initial	Description
15..10	Reserved	R	0x0	
9..0	S2REL[9:0]	R/W	0x3D9	S2RELH[1:0] & S2RELL[7:0]. UART2 Reload Register used for UART2 baud rate generation.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description

7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN1 Register (0xB8)

Bit	Field	Type	Initial	Description
7	EU2RX	R/W	0	UART2 receiver interrupt enable
6	EU2TX	R/W	0	UART2 transmitter interrupt enable
Else				Refer to other chapter(s)

ODCON Register (0xF018)

Bit	Field	Type	Initial	Description
2	UART2OD	R/W	0	UART2 TX/RX open-drain control bit. 0: Disable, Switch UTX2 and URX2 to push-pull mode 1: Enable, Switch UTX2 and URX2 to open-drain mode
Else				Refer to other chapter(s)

23.12 UART3 Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SMODCAL	SMOD3	SMOD2	SMOD1	SMOD0	CD3	CD2	CD1	CD0
S0CON2	BD3	BD2	BD1	BD0	TEN3	TEN2	TEN1	TEN0
S3CON	S3M0	S3M1	S3M20	REN3	TB83	RB83	TI3	RI3
S3BUF	S3BUF7	S3BUF6	S3BUF5	S3BUF4	S3BUF3	S3BUF2	S3BUF1	S3BUF0
S3RELH	-	-	-	-	-	-	S3REL9	S3REL8
S3RELL	S3REL7	S3REL6	S3REL5	S3REL4	S3REL3	S3REL2	S3REL1	S3REL0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN2	EU3RX	EU3TX	-	-	-	ET2	EADC	ELVD
ODCON	-	-	-	SPI0OD	URT3OD	URT2OD	URT1OD	URT0OD

SMODCAL Register (0x95)

Bit	Field	Type	Initial	Description
7	SMOD3	R/W	0	UART3 baud rate control. In UART mode 0: Unused. In UART mode 1, 3: The baud rate generated as the equation in section 23.7 (Baud Rate Control). In UART mode 2:

				0: Fcpu/64 1: Fcpu/32
3	CD3	R/W	0	UART3 clock divider 0: 16-clocks for a cycle 1: 14-clocks for a cycle
Else				Refer to other chapter(s)

S0CON2 Register (0x96)

Bit	Field	Type	Initial	Description
7	BD3	R/W	0	UART3 Baud rate generators selection (mode 1, 3) 0: Timer 1 overflow period 1: Controlled by S3RELH and S3RELL registers
3	TEN3	R/W	0	UART3 TX enable bit 0: Disable 1: Enable
Else				Refer to other chapter(s)

S3CON Register (0xC4)

Bit	Field	Type	Initial	Description
7..6	S3M[0:1]	R/W	00	UART3 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	S3M20	R/W	0	Multiprocessor communication (mode 2, 3) 0: Disable 1: Enable
4	REN3	R/W	0	UART3 module (and reception function) 0: Disable for power saving* 1: Enable for UART operating
3	TB83	R/W	0	The 9th bit transmission data (mode 2, 3)
2	RB83	R/W	0	The 9th bit data from reception
1	TI3	R/W	0	UART3 interrupt flag of transmission
0	RI3	R/W	0	UART3 interrupt flag of reception

✷ ***Note: TI2 and RI2 are clear by software when interrupt is enabled.***

S3BUF Register (0xC5)

Bit	Field	Type	Initial	Description
7..0	S3BUF[7:0]	R/W	0x00	Action of writing data triggers UART3 communication (LSB first). Reception data is available to read by the end of packages.

S3RELH/S3RELL Registers (S3RELH: 0xC7, S3RELL: 0xC6)

Bit	Field	Type	Initial	Description
15..10	Reserved	R	0x0	
9..0	S3REL[9:0]	R/W	0x3D9	S3RELH[1:0] & S3RELL[7:0]. UART3 Reload Register used for UART3 baud rate generation.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN2 Register (0xC8)

Bit	Field	Type	Initial	Description
7	EU3RX	R/W	0	UART3 receiver interrupt enable
6	EU3TX	R/W	0	UART3 transmitter interrupt enable
Else				Refer to other chapter(s)

ODCON Register (0xF018)

Bit	Field	Type	Initial	Description
3	UART3OD	R/W	0	UART3 TX/RX open-drain control bit. 0: Disable, Switch UTX3 and URX3 to push-pull mode 1: Enable, Switch UTX3 and URX3 to open-drain mode
Else				Refer to other chapter(s)

24 I2C

The I2C is a serial communication interface for data exchanging from one MCU to one MCU or other hardware peripherals. The device can transmit data as a master or a slave with two bi-directional IO, SDA (Serial data line) and SCL (Serial clock line).

When a master transmit data to a slave, it's called "WRITE" operation; when a slave transmit data to a master, it's called "READ" operation. It also supports multi-master communication and keeps data transmission correctly by an arbitration method to decide one master has the control on bus and transmit its data.

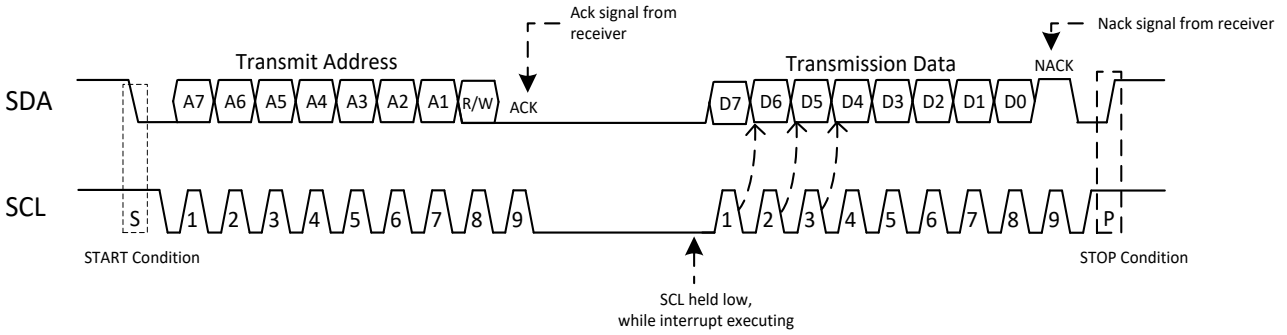
- Master Tx, Rx Mode
- Slave Tx, Rx mode (with general address call) for multiplex slave in single master situation.
- 2-wire synchronous data transfer/receiver.
- Support 100K/400K clock rate.

24.1 I2C Protocol

I2C transmission structure includes a START(S) condition, 8-bit address byte, one or more data byte and a STOP (P) condition. START condition is generated by master to initial any transmission.

Data is transmitted with the Most Significant Bit (MSB) first. In address byte, the higher 7-bit is address bit and the lowest bit is data direction (R/W) bit. When R/W=0, it assigns a "WRITR" operation. When R/W=1, it assigns a "READ" operation.

After each byte is received, the receiver (a master or a slave) must send an acknowledge (ACK). If transmitter can't receive an ACK, it will recognize a not acknowledge (NACK). In WRITE operation, the master will transmit data to the slave and then waits for ACK from slave. In READ operation, the slave will transmit data to the master and then waits for ACK from master. In the end, the master will generate a STOP condition to finish transmission.

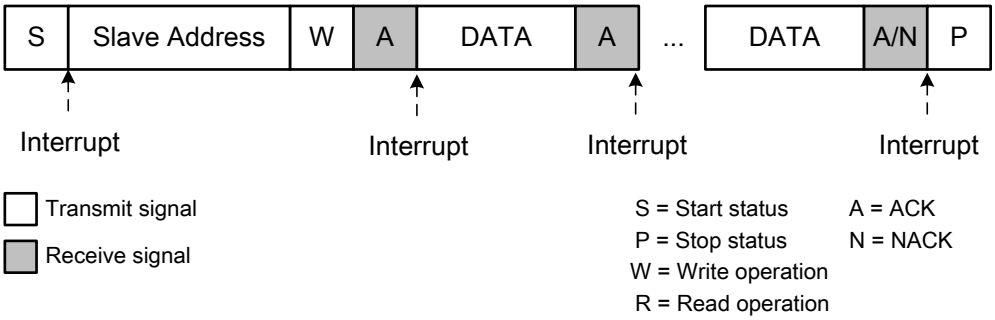


24.2 I2C Transfer Modes

The I2C can operate as a master/slave to execute the 8-bit serial data transmission/reception operation. Thus, the module can operate in one of four modes: Master Transmitter, Master Receiver, Slave Transmitter and Slave Receiver.

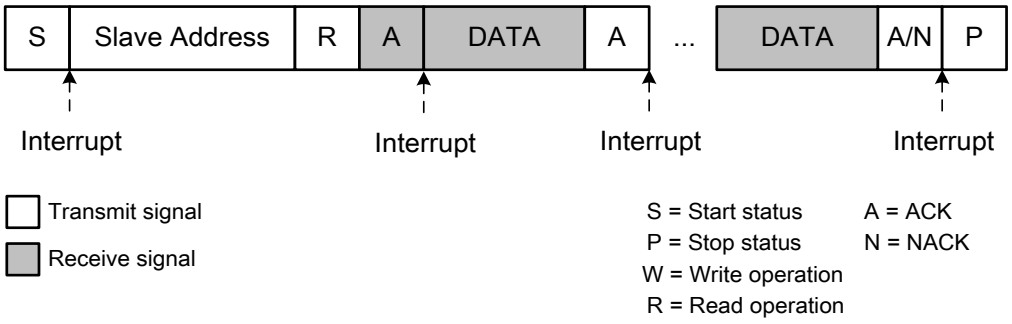
24.2.1 Master Transmitter Mode

The master transmits information to the slave. The serial data is output via SDA while the serial clock is output on SCL. Data transmission starts via generate a START(S) signal. After the START signal, the specific address byte of slave device is sent. The address byte includes 7-bit address bit and an 8th data direction (R/W) bit. The R/W is set “0” to enable the master transmission. In the following, the master transmits one or more data byte to the slave. After each data is transmitted, the master waits for the acknowledge (ACK) from the slave. In the end, the master generates a STOP (P) signal to terminate the data transmission.



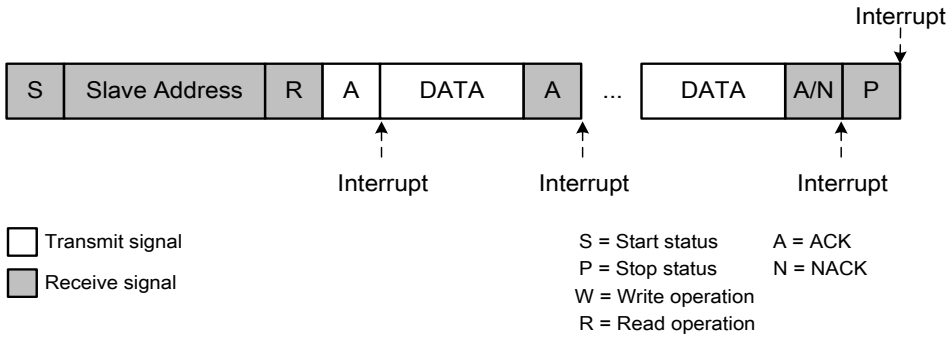
24.2.2 Master Receiver Mode

The master receives the information from the slave. The serial data input via SDA while the serial clock output on SCL. Data reception starts via generate a START(S) signal. After the START signal, the specific address byte of slave device is sent. The address byte includes 7-bit address bit and an 8th data direction (R/W) bit. The R/W is set “1” to enable the master reception. In the following, the master receives one or more data byte from the slave. After each data is received, the master generates the acknowledge (ACK) or not acknowledge (NACK) to the slave via the status of AA bit. In the end, the master generates a STOP (P) signal to terminate the data transmission.



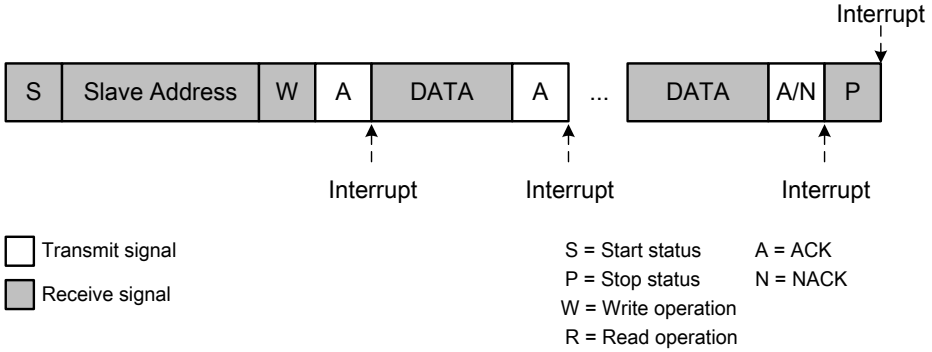
24.2.3 Slave Transmitter Mode

The slave transmits information to the master. The serial data output via SDA while the serial clock input on SCL. Data transmission starts via receive a START(S) signal from the master. After the START signal, the specific address byte of slave device is received. The address byte includes 7-bit address bit and an 8th data direction (R/W) bit. The R/W is set “1” to enable the slave transmission. If the received address byte match the address in I2CADR register, the slave generate an acknowledge (ACK). Otherwise, if general call address condition is set (GC=1), the slave also generate an acknowledge (ACK) after general call address (0x00) is received. In the following, the slave transmits one or more data byte to the master. After each data is transmitted, the slave waits for the acknowledge (ACK) from the master. In the end, the slave receives a STOP (P) signal from the master to terminate the data transmission.



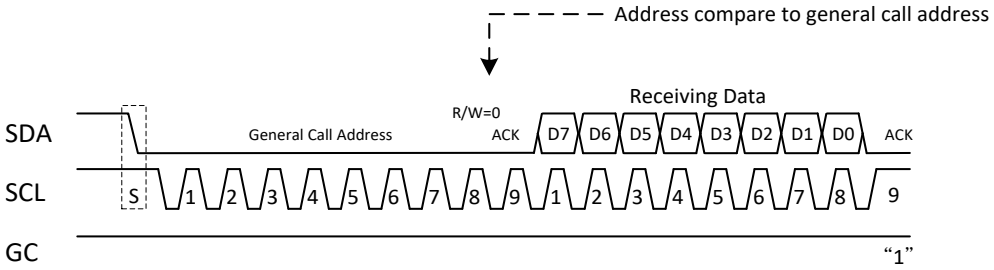
24.2.4 Slave Receiver Mode

The slave receives information from the master. Both the serial data and the serial clock are input on SDA and SCL. Data reception starts via receive a START(S) signal from the master. After the START signal, the specific address byte of slave device is received. The address byte includes 7-bit address bit and an 8th data direction (R/W) bit. The R/W is set “0” to enable the slave reception. If the received address byte match the address in I2CADR register, the slave generate an acknowledge (ACK). Otherwise, if general call address condition is set (GC=1), the slave also generate an acknowledge (ACK) after general call address (0x00) is received. In the following, the slave receives one or more data byte from the master. After each data is receives, the slave generates the acknowledge (ACK) or not acknowledge (NACK) to the master via the status of AA bit. In the end, the slave receives a STOP (P) signal from the master to terminate the data transmission.



24.3 General Call Address

In I2C bus, the first 7-bit is the slave address. Only the address matches slave address, the slave will response an ACK. The exception is the general call address which can address all slave devices. When this address occur, all devices should response an acknowledge (ACK). The general call address is a special address which is reserved as all “0” of 7-bit address. The general call address function is control by GC bit. Set this bit will enable general call address and clear it will disable. When GC=1, the general call address will be recognized. When GC=0, the general call address will be ignored.



24.4 Serial Clock Generator

In master mode, the SCL clock rate generator’s is controlled by CR[2:0] bit of I2CCON register.

When CR[2:0]=000~011, SCL clock rate is from internal clock generator.

$$\text{SCL Clock Rate} = \frac{\text{Fhosc}}{\text{Prescaler}} (\text{Prescaler} = 320 \sim 40)$$

When CR[2:0]=1XX, SCL clock rate is from Timer 1 overflow rate.

$$\text{SCL Clock Rate} = \frac{\text{Timer 1 Overflow}}{8}$$

The table below shows the clock rate under different setting.

CR2	CR1	CR0	Fhosc=4M	Fhosc=8M	Fhosc=16M	Fhosc=32M	Clock Divider
0	0	0	100	200	400	-	40
0	0	1	50	100	200	400	80
0	1	0	25	50	100	200	160
0	1	1	12.5	25	50	100	320
1	X	X	(Timer 1 overflow rate)/8				

✷ ***Note:***

1. When I2C function is enabled, SDA/SCL pins switch to I2C pins’ mode by hardware.

2. When clock generator source is T1 overflow rate, the max counter value is 0xF9. (Only supports 0x00~0xF9).

24.5 Synchronization and Arbitration

In multi-master condition, more than one master may transmit on bus in the same time. It must be decided which master has the control of bus and complete its transmission. Clock synchronization and arbitration are used to configure multi-master transmission. Clock synchronization is executed by synchronizing the SCL signal with anther devices.

When two masters want to transmit data in the same, the clock synchronization will start by the High to Low transition on the SCL. If master 1 clock set LOW first, it holds the SCL in LOW status until the clock transit to HIGH status. However, if anther master clock still keep LOW status, the Low to High transition of master 1 may not change SCL status (SCL keep LOW). In the other word, SCL keep LOW by the master with the longest clock time in LOW status. The SCL will transit from LOW to HIGH when the all devices clock transit to HIGH status. In the duration, the master1 will keep in HIGH status and wait for SCL transition (from LOW to HIGH), then continue its transmission. After clock synchronization, all devices clock and SCL clock are the same. Arbitration is used to decide which master can complete its transmission by SDA signal. Two masters may send out a START condition and transmit data on bus in the same time. They may influence by each other. Arbitration will force one master to lose the control on bus. Data transmission will keep until master output different data signal. If one master transmits HIGH status and anther master transmits LOW status, the SDA will be pull low. The master output High will detect the different with SDA and lose the control on bus. The mater with LOW status wins the bus control and continues its transmission. There is no data miss during arbitration.

24.6 System Management Bus Extension

The optional System Management Bus (SMBus) protocol hardware supports 3 types timeout detection: (1) Tmext Timeout Detection: The cumulative stretch clock cycles within one byte. (2)Tsext Timeout Detection: The cumulative stretch clock cycles between start and stop condition. (3)Timeout Detection: The clock low measurement.

Timeout detection is controlled by SMBSEL and SMBDST registers. The SMBEXE bit of SMBSEL is SMBus extension function enable bit. When SMBEXE=1, SMBus extension function is enabled. Otherwise, Disable SMBus extension function. Timeout type and period setting is controlled by SMBTOP[2:0] and SMBDST. The period of SMBus timeout is controlled by three 16-bit buffers of

Tmext, Tsext and Tout. The equation is as following.

$$\text{Tmext/Tsext/Tout} = \frac{\text{Timeout Period(sec)xFcpu(Hz)}}{1024}$$

Tmext is support by two 8-bit register of Tmext_L and Tmext_H . Tmext_L hold the low byte and Tmext_H hold high byte. Tsext is support by two 8-bit register of Tsext_L and Tsext_H . Tsext_L hold the low byte and Tsext_H hold high byte. Tout is support by two 8-bit register of Tout_L and Tout_H . Tout_L hold the low byte and Tout_H hold high byte.

Type	Time out period	Fhosc=32MHz	
		DEC	HEX
Tmext	5ms	156	9C
Tsext	25ms	781	30D
Tout	35ms	1094	446

By the setting of SMBTOP[2:0] to choose register type (as the table below), and write to register by write data to SMBDST register.

SMBTOP[2:0]	SMBDST	Description
000	Tmext_L	Select the low byte of Tmext register.
001	Tmext_H	Select the high byte of Tmext register.
010	Tsext_L	Select the low byte of Tsext register.
011	Tsext_H	Select the high byte of Tsext register.
100	Tout_L	Select the low byte of Tout register.
101	Tout_H	Select the high byte of Tout register.

When the SMBus extension function is enabled the lower 3-bit of I2CSTA hold the information about time out as the table below.

I2CSTA	Description
XXXX X000	No timeout errors.
XXXX XXX1	Tout timeout error.
XXXX XX1X	Tsext timeout error.
XXXX X1XX	Tmext timeout error.

24.7 Power Saving

The I2C module has clock gating function for saving power. When ENS1 bit is 0, the I2C module internal clocks are halted to reduce power consumption. Conversely, when ENS1 bit is 1, I2C internal clocks are run, and registers can access. The ENS1 bit must be set to 1, before the initial setting I2C.

24.8 I2C Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CDAT	I2CDAT7	I2CDAT6	I2CDAT5	I2CDAT4	I2CDAT3	I2CDAT2	I2CDAT1	I2CDAT0
I2CADR	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	GC
I2CCON	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
I2CSTA	I2CSTA7	I2CSTA6	I2CSTA5	I2CSTA4	I2CSTA3	I2CSTA2	I2CSTA1	I2CSTA0
SMBSEL	SMBEXE	-	-	-	I2CMX	SMBTOP2	SMBTOP1	SMBTOP0
SMBDST	SMBD7	SMBD6	SMBD5	SMBD4	SMBD3	SMBD2	SMBD1	SMBD0
IEN0	EAL	EX4	EX3	EX2	ET1	EX1	ET0	EX0
IEN1	EU2RX	EU2TX	EU1RX	EU1TX	EU0RX	EU0TX	ESPI	EI2C

I2CDAT Register (0xDA)

Bit	Field	Type	Initial	Description
7:0	I2CDAT[7:0]	R/W	0x00	The I2CDAT register contains a byte to be transmitted through I2C bus or a byte which has just been received through I2C bus. The CPU can read from and write to this 8-bit, directly addressable SFR while it is not in the process of byte shifting. The I2CDAT register is not shadowed or double buffered so the user should only read I2CDAT when an I2C interrupt occurs.

I2CADR Register (0xDB)

Bit	Field	Type	Initial	Description
7:1	I2CADR[6:0]	R/W	0x00	I2C slave address
0	GC	R/W	0	General call address (0X00) acknowledgment 0: ignored 1: recognized

I2CCON Register (0xDC)

Bit	Field	Type	Initial	Description
7,1,0	CR[2:0]	R/W	0	I2C clock rate 000: Fhosc/40 001: Fhosc /80 010: Fhosc /160 011: Fhosc /320 1XX: Timer 1 overflow-period/8
6	ENS1	R/W	0	I2C functionality 0: Disable for power saving* 1: Enable for I2C operating
5	STA	R/W	0	START flag 0: No START condition is transmitted. 1: A START condition is transmitted if the bus is free.
4	STO	R/W	0	STOP flag 0: No STOP condition is transmitted. 1: A STOP condition is transmitted to the I2C bus in master mode.
3	SI	R/W	0	Serial interrupt flag The SI is set by hardware when one of 25 out of 26 possible I2C states is entered. The only state that does not set the SI is state F8h, which indicates that no relevant state information is available. The SI flag must be cleared by software. In order to clear the SI bit, ‘0’ must be written to this bit. Writing a ‘1’ to SI bit does not change value of the SI.
2	AA	R/W	0	Assert acknowledge flag 0: A NACK will be returned when a byte has received 1: An ACK will be returned when a byte has received

* When ENS1 bit is 0, I2C relevant register are unable to access, and the module internal clocks are halted.

I2CSTA Register (0xDD)

Bit	Field	Type	Initial	Description
7:3	I2CSTA[7:3]	R	11111	I2C Status Code
2..0	I2CSTA[2:0]	R	000	SMBus Status Code

I2C status code and status

Mode	Status Code	Status of the I2C	Application software response					Next action taken by I2C hardware
			To/from I2CDAT	TO I2CCON				
				STA	STO	SI	AA	
Master Transmitter/ Receiver	08H	A START condition has been transmitted	Load SLA+R/W	X	0	0	X	SLA+R/W will be transmitted; ACK will be received
	10H	A repeated START condition has been transmitted.	Load SLA+R/W	X	0	0	X	SLA+R/W will be transmitted; ACK will be received
			Load SLA+R/W					SLA+W will be transmitted; I2C will be switched to MST/TRX mode.
Master Transmitter	18H	SLA+W has been transmitted; ACK has been received	Load data byte	0	0	0	X	Data byte will be transmitted; ACK will be received.
			No action	1	0	0	X	Repeated START will be transmitted.
			No action	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
			No action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
	20H	SLA+W has been transmitted; not ACK has been received	Load data byte*	0	0	0	X	Data byte will be transmitted; ACK will be received.
			No action	1	0	0	X	Repeated START will be transmitted.
			No action	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
			No action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
	28H	Data byte in I2CDAT has been transmitted; ACK has been received	Load data byte	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
			No action	1	0	0	X	Repeated START will be transmitted.
			No action	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
			No action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
	30H	Data byte in I2CDAT has been transmitted; not ACK has been received	Load data byte*	0	0	0	X	Data byte will be transmitted; ACK will be received.
			No action	1	0	0	X	Repeated START will be transmitted.
			No action	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
			No action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
Master Receiver	40H	SLA+R has been transmitted; ACK has been received	No action	0	0	0	0	Data byte will be received; not ACK will be returned
			No action	0	0	0	1	Data byte will be received; ACK will be returned
	48H	SLA+R has been transmitted; not ACK has been received	No action	1	0	0	X	Repeated START condition will be transmitted
			No action	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
			No action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset
	50H	Data byte has been received; ACK has been returned	Read data byte	0	0	0	0	Data byte will be received; not ACK will be returned
			Read data byte	0	0	0	1	Data byte will be received; ACK will be returned
	58H	Data byte has been received; not ACK has been returned	Read data byte	1	0	0	X	Repeated START condition will be transmitted
			Read data byte	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
			Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset

Mode	Status Code	Status of the I2C	Application software response					Next action taken by I2C hardware
			To/from I2CDAT	TO I2CCON				
				STA	STO	SI	AA	
Slave Receiver	60H	Own SLA+W has been received; ACK has been returned	No action	X	0	0	0/1	Data byte will be received and not ACK/ACK will be returned
	68H	Arbitration lost in SLA+R/W as master; own SLA+W has been received, ACK returned	No action	X	0	0	0/1	Data byte will be received and not ACK/ACK will be returned
	70H	General call address (00H) has been received; ACK has been returned	No action	X	0	0	0/1	Data byte will be received and not ACK/ACK will be returned
	78H	Arbitration lost in SLA+R/W as master; general call address has been received, ACK returned	No action	X	0	0	0/1	Data byte will be received and not ACK/ACK will be returned
	80H	Previously addressed with own SLV address; DATA has been received; ACK returned	Read data byte	X	0	0	0/1	Data byte will be received and not ACK/ACK will be returned
	88H		Read data byte	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address

		Previously addressed with own SLA; DATA byte has been received; not ACK returned	Read data byte	0	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized
			Read data byte	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address; START condition will be transmitted when the bus becomes free
			Read data byte	1	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized; START condition will be transmitted when the bus becomes free
	90H	Previously addressed with general call address; DATA has been received; ACK returned	Read data byte	X	0	0	0/1	Data byte will be received and not ACK/ACK will be returned
	98H	Previously addressed with general call address; DATA has been received; not ACK returned	Read data byte	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address
			Read data byte	0	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized
			Read data byte	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address; START condition will be transmitted when the bus becomes free
			Read data byte	1	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized; START condition will be transmitted when the bus becomes free
	A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX	No action	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address
			No action	0	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized
			No action	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address; START condition will be transmitted when the bus becomes free
			No action	1	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized; START condition will be transmitted when the bus becomes free
Slave Transmitter	A8H	Own SLA+R has been received; ACK has been returned	Load data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received
			Load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.
	B0H	Arbitration lost in SLA+R/W as master; own SLA+R has been received, ACK has been returned.	Load data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received
			Load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.
	B8H	Data byte has been transmitted; ACK will be received.	Load data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received
			Load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.
	C0H	Data byte has been transmitted; not ACK has been received.	No action	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address.
			No action	0	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized.
			No action	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address; START condition will be transmitted when the bus becomes free.
			No action	1	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized; START condition will be transmitted when the bus becomes free.
	C8H	Last data byte has been transmitted; ACK has been received.	No action	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address.
			No action	0	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized.
			No action	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address; START condition will be transmitted when the bus becomes free.
			No action	1	0	0	1	Switched to not addressed SLV mode; own SLA or general call address will be recognized; START condition will be transmitted when the bus becomes free.
Miscellaneous	F8H	No relevant state information available; SI=0	No action	No action				Wait or proceed current transfer
	38H	Arbitration lost	No action	0	0	0	X	I2C will be released; A start condition will be transmitted.
			No action	1	0	0	X	When the bus becomes free. (enter to a master mode)
	00H	Bus error during MST or selected slave modes	No action	0	1	0	X	Only the internal hardware is affected in the MST or addressed SLV modes. In all cases, the bus is released and I2C is switched to the not addressed SLV mode. STO flag is reset.

"SLA" means slave address, "R" means R/W=1, "W" means R/W=0

*For applications where NACK doesn't mean the end of communication.

SMBSEL Register (0xDE)

Bit	Field	Type	Initial	Description
7	SMBEXE	R/W	0	SMBus extension functionality 0: Disable 1: Enable
Else	Reserved	R/W	0	
3	I2CMX	R/W	0	I2C IO select bit. 0:I2C SCL is P2.3/ SDA is P2.4. 1: I2C SCL(1) is P4.4/ SDA(1) is P4.5.
2..0	SMBTOP[2:0]	R/W	000	SMBus timeout register

SMBDST Register (0xDF)

Bit	Field	Type	Initial	Description
7..0	SMBD[7:0]	R/W	0x00	This register is used to provide a read/write access port to the SMBus timeout registers. Data read or written to that register is actually read or written to the Timeout Register which is pointed by the SMBSEL register.

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN1 Register (0xB8)

Bit	Field	Type	Initial	Description
0	EI2C	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

25 SPI

The SPI a serial communicate interface for data exchanging from one MCU to one MCU or other hardware peripherals. It is a simple 8-bit interface without a major definition of protocol, packet or control bits. The SPI transceiver includes three pins, clock (SCK), data input and data output (MISO/ MOSI) to send data between master and slave terminals. An optional slave select pin (SSN) can be enabled by register in slave mode. The SPI interface builds in 4-mode which are the clock idle status and the clock phases. Master Tx, Rx Mode

- Full-duplex, 3-wire synchronous data transfer.
- Master (SCK is clock output) or Slave (SCK is clock input) operation.
- Seven SPI Master baud rates.
- Slave Clock rate up to Fcpu/8.
- 8-bit data transmitted MSB first, LSB last.
- Serial clock with programmable polarity and phase.
- Master Mode fault error flag with MCU interrupt capability.
- Write collision flag protection.

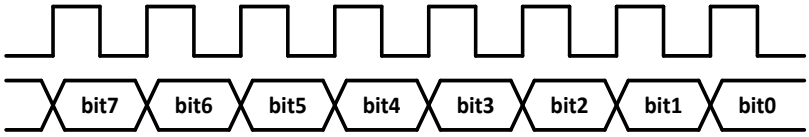
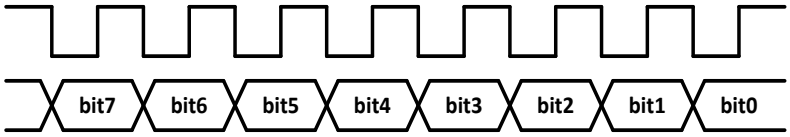
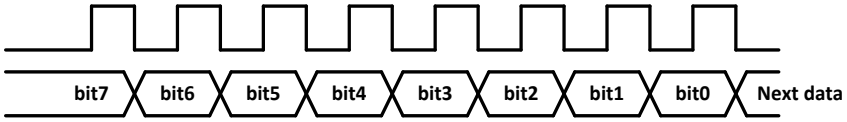
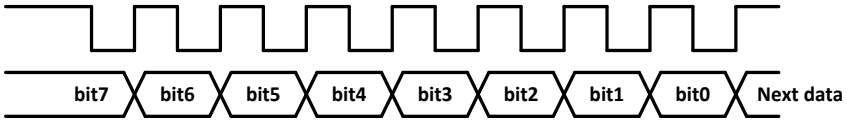
25.1 SPI Operation

The SPCON register can control SPI operating function, such as: transmit/receive, clock rate, data transfer direction, SPI clock idle status and clock control phase and enable this circuit. This SPI circuit will transmit or receive 8-bit data automatically by setting SPEN in SPCON register and write or read SPDAT register.

CPOL bit is designed to control SPI clock idle status. CPHA bit is designed to control the clock edge direction of data receive. CPOL and CPHA bits decide the SPI format. The SPI data transfer direction is MSB bit to LSB bit.

The SPI supports 4-mode format controlled by CPOL and CPHA bits. The edge direction is “Data Transfer Edge”. When setting rising edge that means to receive and transmit one bit data at SCK rising edge, and data transition is at SCK falling edge. When setting falling edge, that means to receive and transmit one bit data at SCK falling edge, and data transition is at SCK rising edge.

“CPHA” is the clock phase bit controls the phase of the clock on which data is sampled. When CPHA=1, the SCK first edge is for data transition, and receive and transmit data is at SCK 2nd edge. When CPHA=0, the 1st bit is fixed already, and the SCK first edge is to receive and transmit data. The SPI data transfer timing as following figure:

CPOL	CPHA	Diagrams	Description
0	1		SCK idle status = Low. The transfer first bit = MSB. SCK data transfer edge = Falling edge.
1	1		SCK idle status = High. The transfer first bit = MSB. SCK data transfer edge = Rising edge.
0	0		SCK idle status = Low. The transfer first bit = MSB. SCK data transfer edge = Rising edge.
1	0		SCK idle status = High. The transfer first bit = MSB. SCK data transfer edge = Falling edge.

The SPI supports interrupt function. ESPI is SPI interrupt function control bit. ESPI=0, disable SPI interrupt function. ESPI=1, enable SPI interrupt function. When SPI interrupt function enable, the program counter points to interrupt vector to do SPI interrupt service routine after SPI operating. SPIF is SPI interrupt request flag, and also to be the SPI operating status indicator when ESPI= 0, but cleared by reading the SPSTA, SPDAT registers.

SPI builds in chip selection function to implement SPI multi-device mode. One master communicating with several slave devices in SPI bus, and the chip selection decides the pointed device. The chip selection pin is SSN pin.

The SPI pins also support open-drain structure. The open-drain option is controlled by PnOC bits. When PnOC=0, disable SPI open-drain structure. When PnOC=1, enable SPI open-drain structure. If enable open-drain structure, SPI pins must be set input mode and need external pull-up resistor.

25.2 SPI Master

The SPI master mode has seven types of clock generator from Fcpu/2 to Fcpu/128. Generated clock is outputted through SCK pin and its idle status is controlled by CPOL.

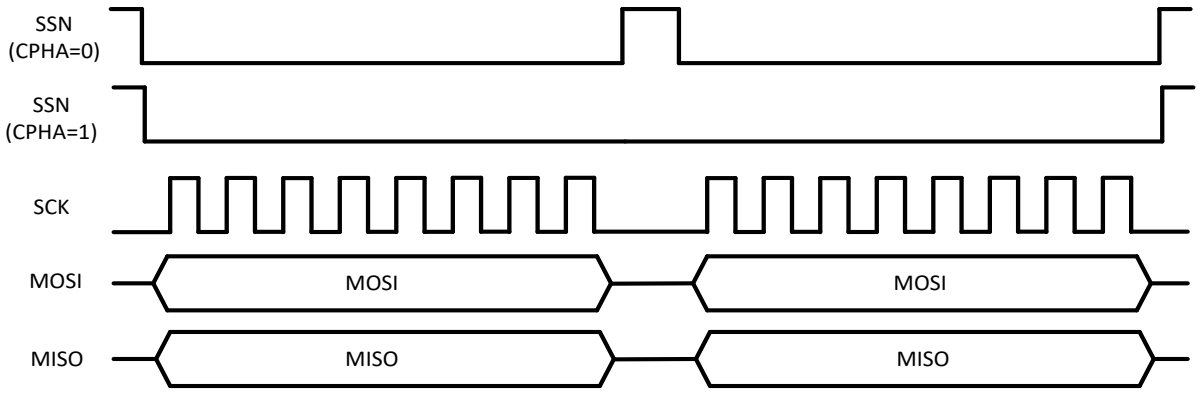
The phase of data input and output is automatically specified by CPHA register. In master mode MOSI pin plays the role of data output, and MISO pin fetches data from slave device. A SPI communication is started by writing SPDAT register; the received data from MISO is available to read after the end of data transmission.

The master mode has two status flags with interrupt function:
SPIF register indicates the end of one byte data communication. An interrupt would be issued at the same time if ESPI bit is enabled.
MODF is issued by SSN low status while transmission. This interrupt source can be masked by setting SSDIS bit.

25.3 SPI Slave

The SPI slave mode monitors SCK pin to control its MISO and MOSI communication. However, the maximum clock rate is limited at Fcpu/8. Slave device(s) are expected to specify its CPOL and CPHA setting as the same configuration of the connected SPI bus.

The slave mode treats MOSI pin as its data input, and MISO pin as its data transmission. By default, the SSDIS register is low which means the slave select pin (SSN) is functional. A SPI communication would be processed if the SSN is low status. Thus, a slave device is suspended if its SSN is high status. But in CPHA = 0, Strictly SSN must follow each 8-bit data needs to be included with falling edge and rising edge, CPHA=1 is not limitation.



✷ ***Note:***

If slave mode with SSN function: essentially to set SSN as input mode.

The slave mode has two status flags with interrupt function:
SPIF indicates the end of one byte data communication. The original SPDAT's value has been transmitted, and the received data from MOSI is ready to be read on SPDAT.
MODF indicates that the slave select pin (SSN) has turned high before a completion of one byte communication. In other word, the last time of SPI communication is broken.

25.4 Power Saving

The SPI module has clock gating function for saving power. When SPEN bit is 0, the SPI module internal clocks are halted to reduce power consumption. Conversely, when SPEN bit is 1, SPI internal clocks are run, and registers can access. The SPEN bit must be set to 1, before the initial setting SPI.

25.5 SPI Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPR2	SPEN	SSDIS	MATR	CPOL	CPHA	SPR1	SPR0
SPSTA	SPIF	WCOL	SSERR	MODF	-	-	-	SPIMX
SPDAT	SPDAT7	SPDAT6	SPDAT5	SPDAT4	SPDAT3	SPDAT2	SPDAT1	SPDAT0
IEN0	EAL	-	-	EX2	ET1	EX1	ET0	EX0
IEN1	-	-	EU1RX	EU1TX	EU0RX	EU0TX	ESPI	EI2C
P6M	P67M	P66M	P65M	P64M	P63M	P62M	P61M	P60M
P4M	P47M	P46M	P45M	P44M	P43M	P42M	P41M	P40M
ODCON	-	-	-	SPI0OD	URT3OD	URT2OD	URT1OD	URT0OD

SPCON Register (0xE2)

Bit	Field	Type	Initial	Description
7,1,0	SPR[2:0]	R/W	000	SPI baud rate generator (master mode only) 000: Fcpu/2 001: Fcpu/4 010: Fcpu/8 011: Fcpu/16 100: Fcpu/32 101: Fcpu/64 110: Fcpu/128 111: reserved
6	SPEN	R/W	0	SPI communication function 0: Disable for power saving* 1: Enable for SPI operating

5	SSDIS	R/W	0	Slave select pin function (MSTR = 0, CPHA = 0 only) 0: Enable slave selection pin (SSN) function 1: Disable slave select pin (SSN) function
4	MSTR	R/W	1	SPI mode 0: Slave mode 1: Master mode
3	CPOL	R/W	0	SCK pin idle status 0: SCK idle low 1: SCK idle high
2	CPHA	R/W	1	Clock phase of data latch control 0: Data latched by the first of clock edge 1: Data latched by the second of clock edge

* When SPEN bit is 0, SPI relevant register are unable to access, and the module internal clocks are halted.

SPSTA Register (0xE1)

Bit	Field	Type	Initial	Description
7	SPIF	R	0	SPI complete communication flag Set automatically at the end of communication Cleared automatically by reading SPSTA, SPDAT registers
6	WCOL	R	0	Write collision flag Set automatically if write SPDAT during communication Cleared automatically by reading SPSTA, SPDAT registers
5	SSERR	R	0	Synchronous slave select pin error Set automatically if SSN error controlling Cleared automatically by clear SPEN
4	MODF	R	0	Mode fault flag
3..1	Reserved	R	000	
0	SPIMX	R/W	0	SPI IO select bit 0: SPI pins are P40, P41, P42 and P43 1: SPI pins are P40, P60, P61 and P62

SPDAT Register (0xE3)

Bit	Field	Type	Initial	Description
7..0	SPDAT[7:0]	R/W	0x00	Master mode: action of writing data triggers SPI communication; reception data is readable after the end of one byte communication (SPIF automatically set).

				Slave mode: written data would be transmitted by SCK input; reception data is available to read after the end of one byte communication (SPIF automatically set).

IEN0 Register (0xA8)

Bit	Field	Type	Initial	Description
7	EAL	R/W	0	Interrupts enable. Refer to Chapter Interrupt
Else				Refer to other chapter(s)

IEN1 Register (0xB8)

Bit	Field	Type	Initial	Description
1	ESPI	R/W	0	Enable SPI interrupt
Else				Refer to other chapter(s)

ODCON Register (0xF018)

Bit	Field	Type	Initial	Description
4	SPI0OD	R/W	0	SPI MOSI/MISO/SCK open-drain control bit. 0: Disable, Switch MOSI/ MISO/SCK to push-pull mode 1: Enable, Switch MOSI/MISO/SCK to open-drain mode
Else				Refer to other chapter(s)

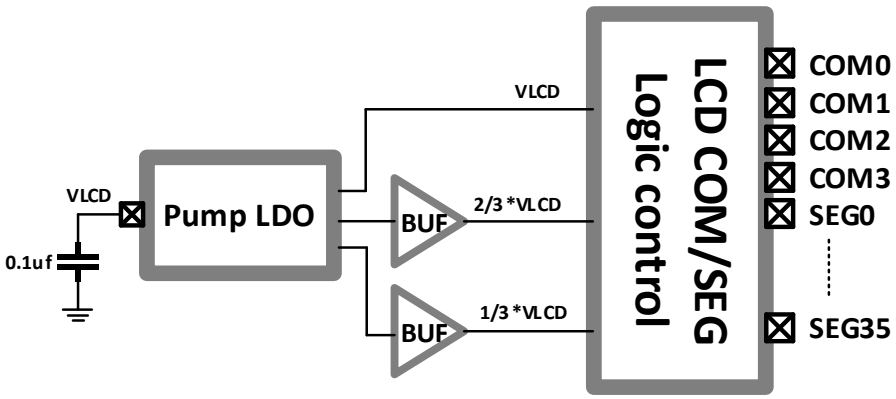
26 LCD

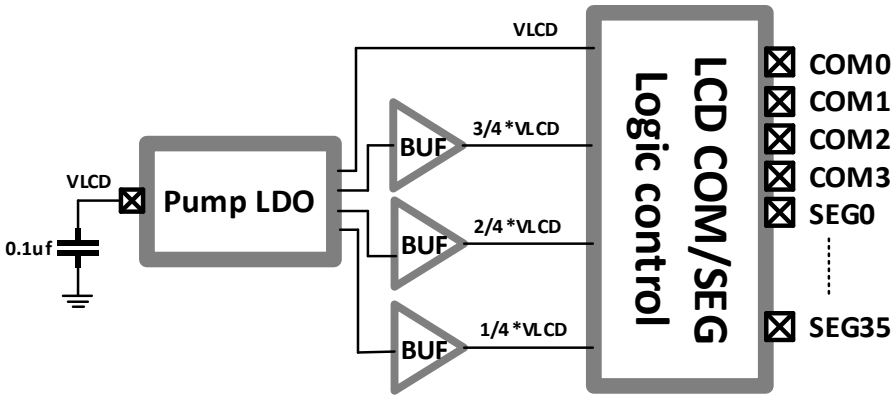
LCD driver is C-type or R-type structures with 4 x 36, 5 x 35, 6 x 34 or 8 x 32. The LCD scan timing is 1/4, 1/5, 1/6 or 1/8 duty with 1/3 bias or 1/4 bias, to drive LCD of 144 dots, 175 dots, 204 dots or 256 dots.

26.1 C-Type LCD

C-type LCD driver can output adjustable VLCD output voltage and adjustable driving power to support diversity of LCD panel. VLCD Pin must connect 0.1uF capacitor to VSS for C-Type LCD driver operation.

- **Stop mode function**: LCD function keeps running in stop mode as LCDEN = 1 & STWK = 1.
- **Low power mode function**: LCD low power function is controlled by BGM bit.

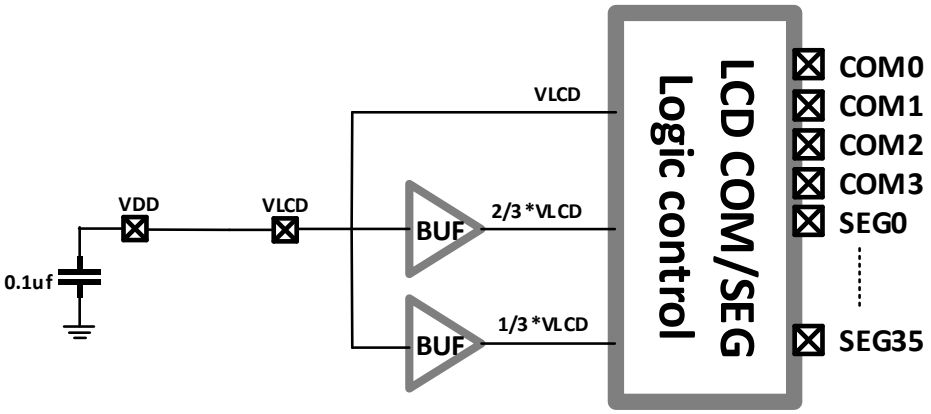


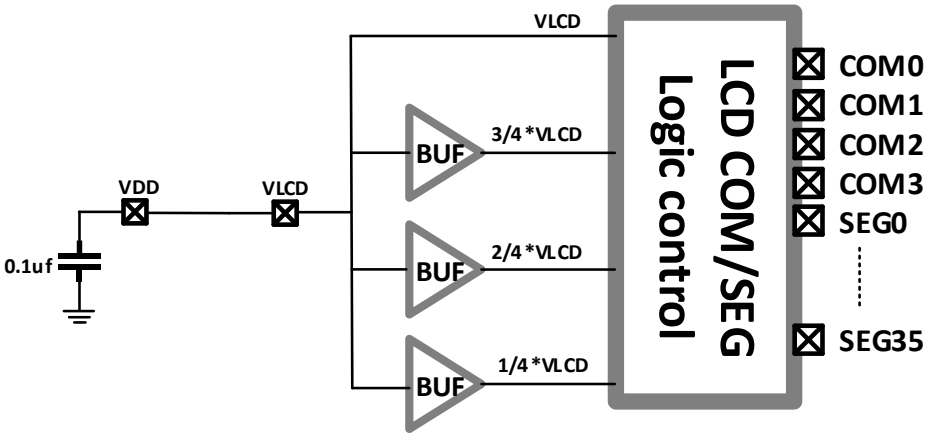


26.2 R-Type LCD

R-type LCD driver can output adjustable VLCD output voltage and adjustable driving power to support diversity of LCD panel. VLCD voltage level is equal to VDD. It is control by RCMOD bit for R-Type LCD driver operation.

- **Stop mode function**: LCD function keeps running in stop mode as LCDEN = 1 & STWK = 1.
- **Low power mode function**: LCD low power function is controlled by BGM bit.





26.3 LCD Timing Control

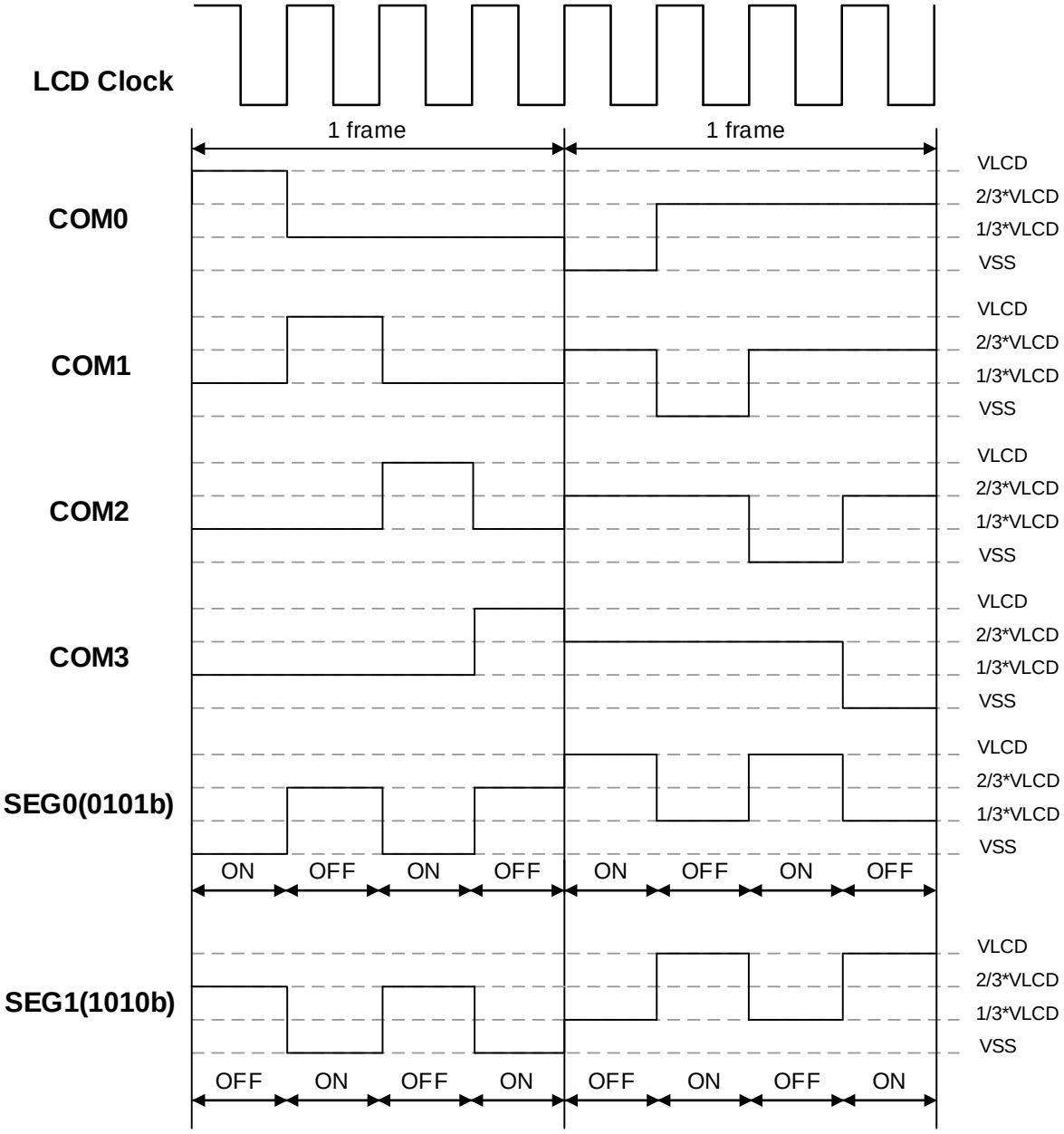
The LCD has two clock source and two clock rates to decide LCD frame rate from 32Hz to 256Hz. The clock source is from internal 32kHz RC or external 32.768kHz oscillator crystal and controlled by code option setting (Low Speed Clock Source).

LCD driver output 4, 5, 6 or 8-com waveform controlled by LCDMODE[1:0] bit, the output frame Rate controlled by LCDRATE bit, which shows in following table:

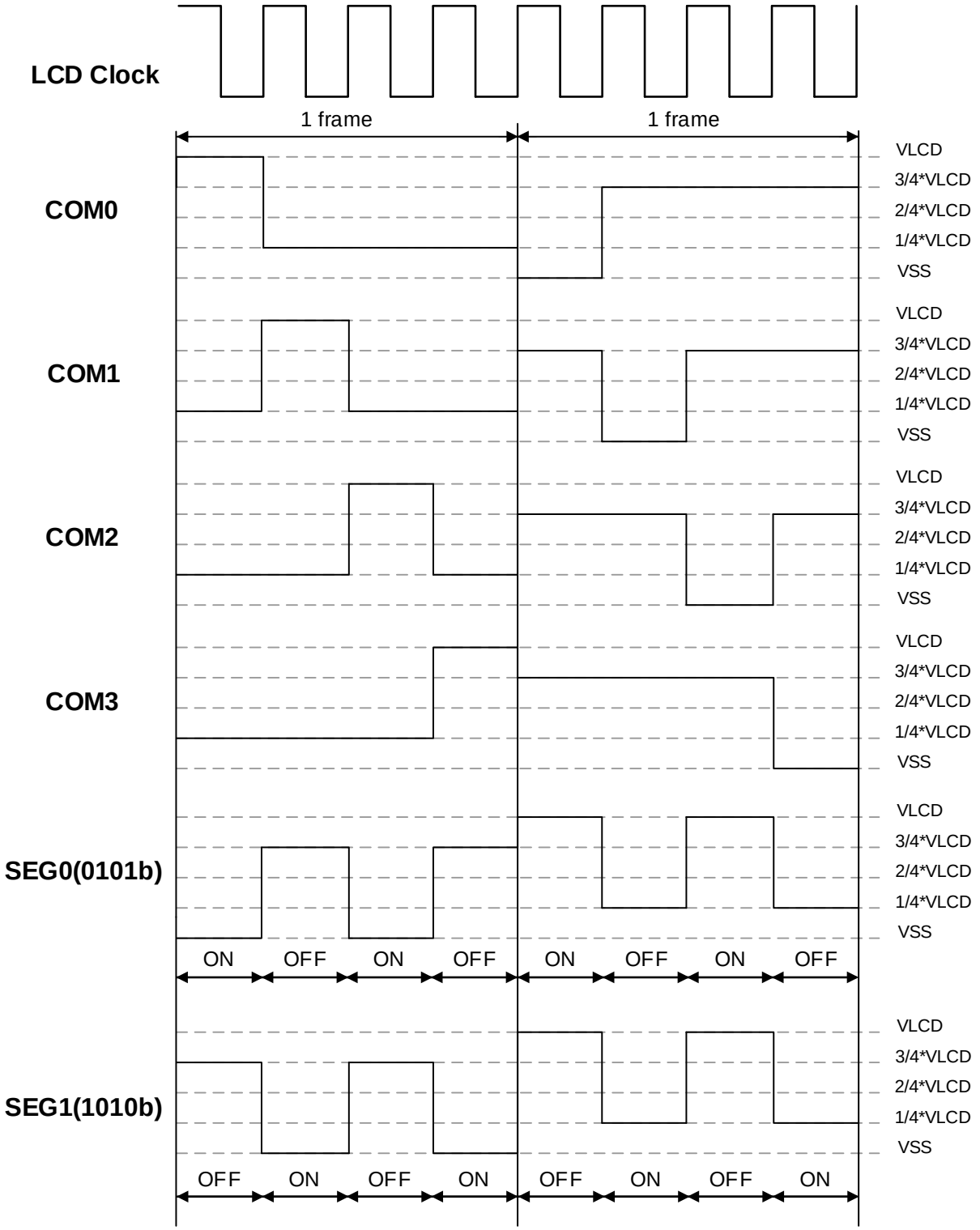
Control Register		LCD Clock (Hz)	Frame Rate (Hz)	Type
LCDRATE[1:0]	LCDMODE[1:0]			
00	00	32KHz / 128 =256	64	4-COM(1/4 duty)
00	01		51	5-COM(1/5 duty)
00	10		43	6-COM(1/6 duty)
00	11		32	8-COM(1/8 duty)
01	00	32KHz / 64 =512	128	4-COM(1/4 duty)
01	01		102	5-COM(1/5 duty)
01	10		85	6-COM(1/6 duty)
01	11		64	8-COM(1/8 duty)
10	00	32KHz / 32 =1024	256	4-COM(1/4 duty)
10	01		205	5-COM(1/5 duty)
10	10		171	6-COM(1/6 duty)
10	11		128	8-COM(1/8 duty)

26.4 LCD Drive Waveform Generation

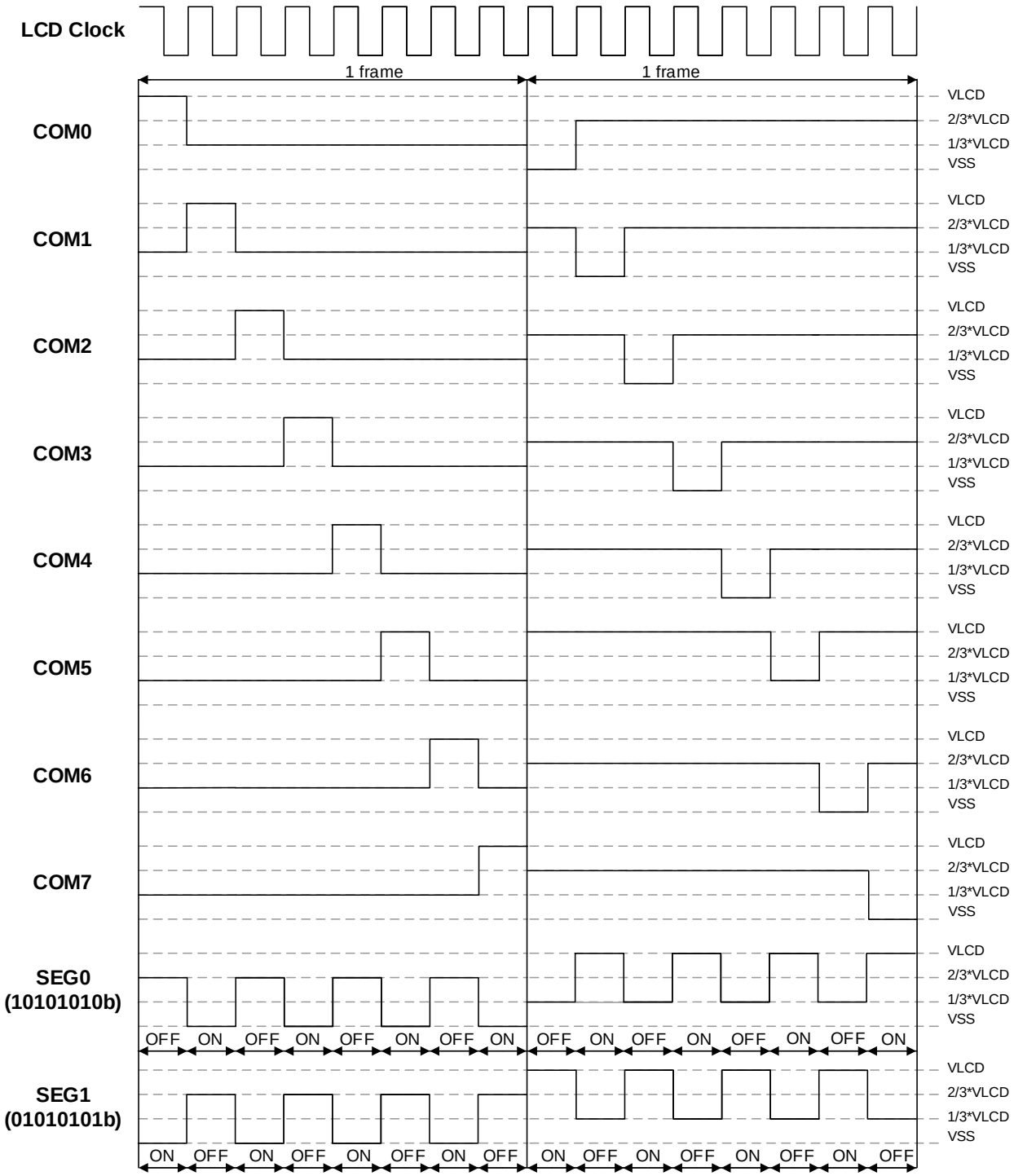
LCD Drive Waveform, 1/4 duty, 1/3 bias :



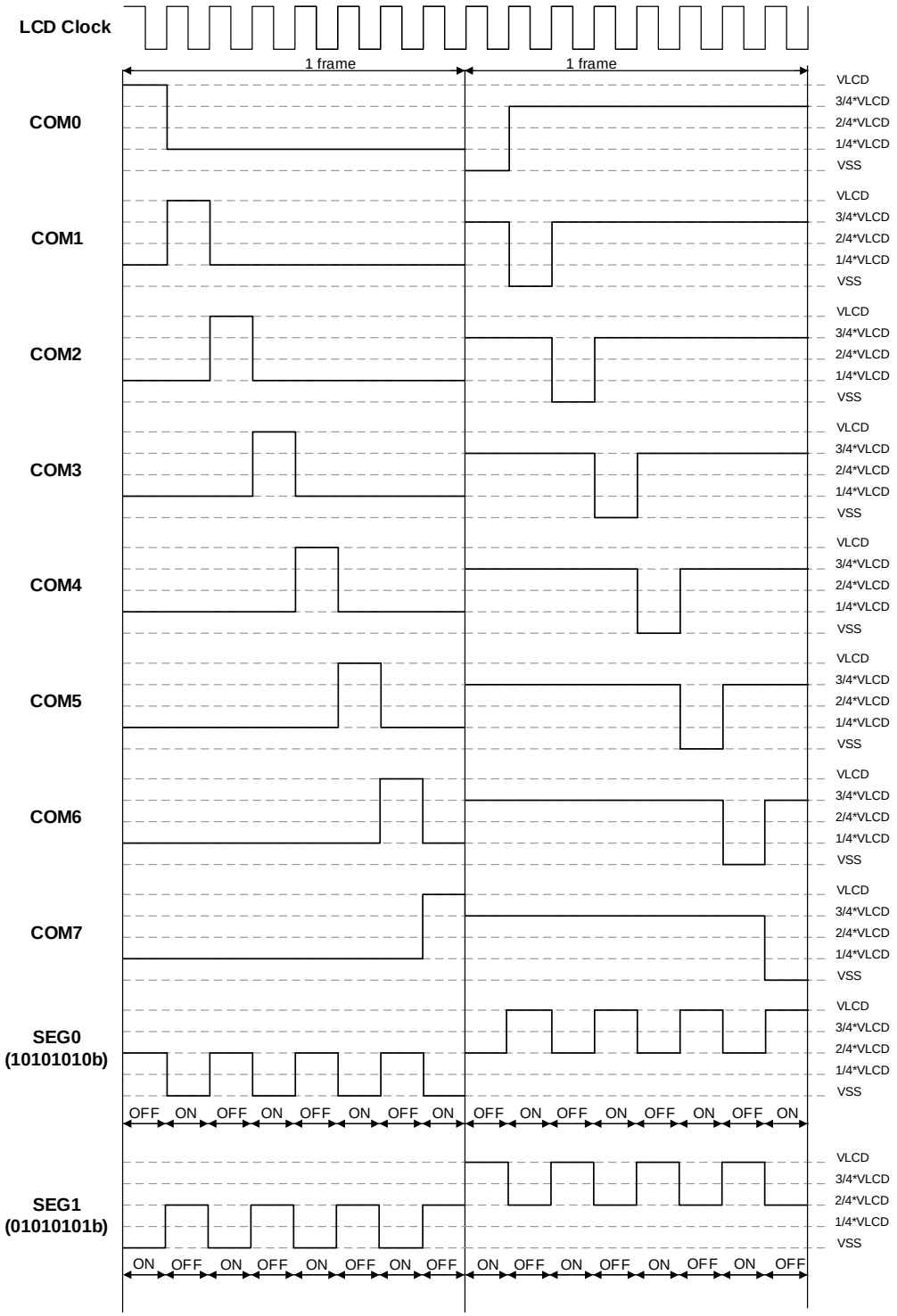
LCD Drive Waveform, 1/4 duty, 1/4 bias :



LCD Drive Waveform, 1/8 duty, 1/3 bias :



LCD Drive Waveform, 1/8 duty, 1/4 bias :



26.5 LCD Low Power Mode

Definition of DUTYA[1:0] :

The LCD C type supports low power mode, which can be enabled or disabled using the BGM bit. When LCD C type is in Normal Mode, the waveform duration of each LCD clock cycle =100%. In low power mode, the DUTYA[1:0] determine the duration for which the waveform remains active within each COM/SEG time unit. This duration setting is determined by the LCD clock source (e.g., 32 kHz); therefore, different LCD clock sources will result in different duty cycle ratios

LCD Clock	Low Power Duty	Duty (%)
LCDRATE[1:0] = 00/01/10	Duty[1:0] = 00/01/10/11	
256Hz (128T)	4T	3.13%
	6T	4.69%
	8T	6.25%
	16T	12.50%
512Hz (64T)	4T	6.25%
	6T	9.38%
	8T	12.50%
	16T	25.00%
1024Hz (32T)	4T	12.50%
	6T	18.75%
	8T	25.00%
	16T	50.00%

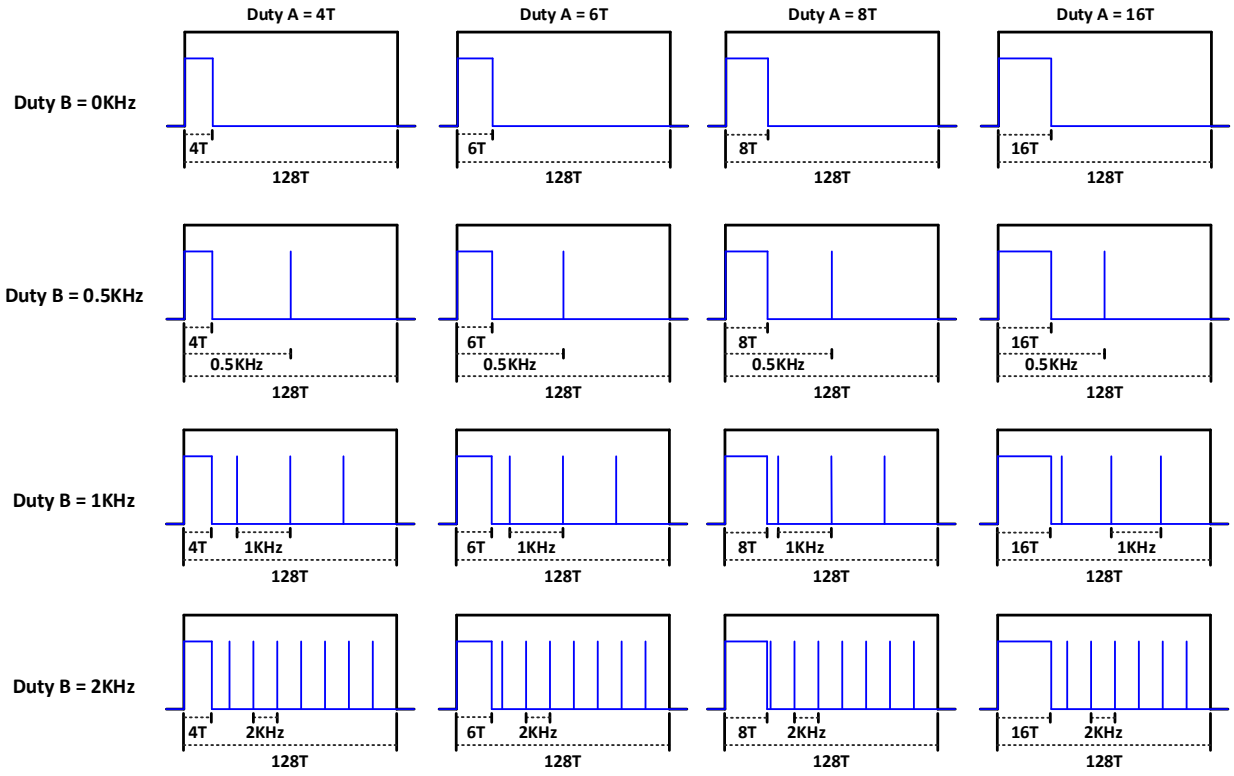
Note : T = LCD Clock Source = 1/(ILRC or L'XTAL) , not LCD Clock

Definition of DUTYB[1:0] :

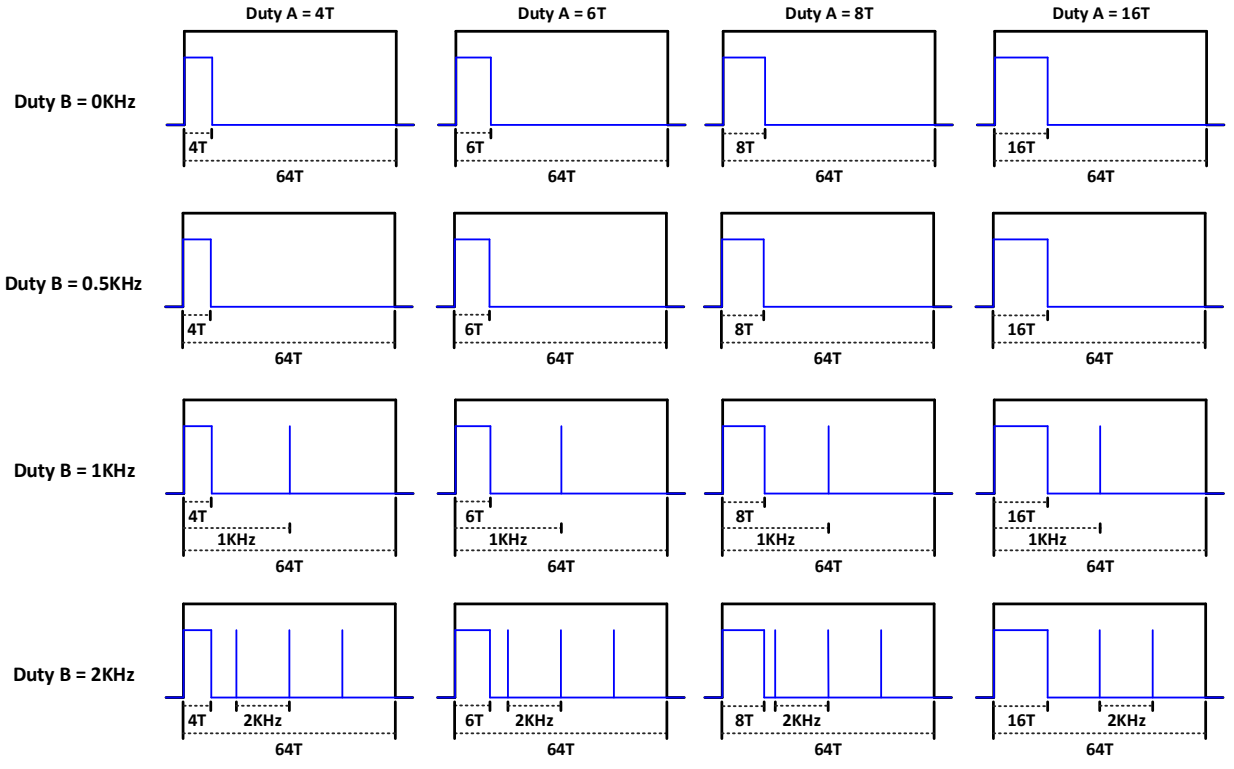
DUTYB[1:0] is used to control the period of the replenish pulse. Under the same DUTYB[1:0] setting, different LCD clock frequencies (256 Hz / 512 Hz / 1024 Hz) will result in different numbers of replenish pulses.

LCD Clock	Low power Duty	Pump Pulse Replenish Period DUTYB[1:0]			
LCDRATE[1:0]	DUTYA[1:0]	00=Disable	01=64T(0.5KHz)	10=32T(1KHz)	11=16T(2KHz)
256Hz (128T)	4T	N/A	1	3	7
	6T		1	3	7
	8T		1	3	7
	16T		1	3	6
512Hz (64T)	4T		0	1	3
	6T		0	1	3
	8T		0	1	3
	16T		0	1	2
1024Hz (32T)	4T		0	0	1
	6T		0	0	1
	8T		0	0	1
	16T		0	0	0

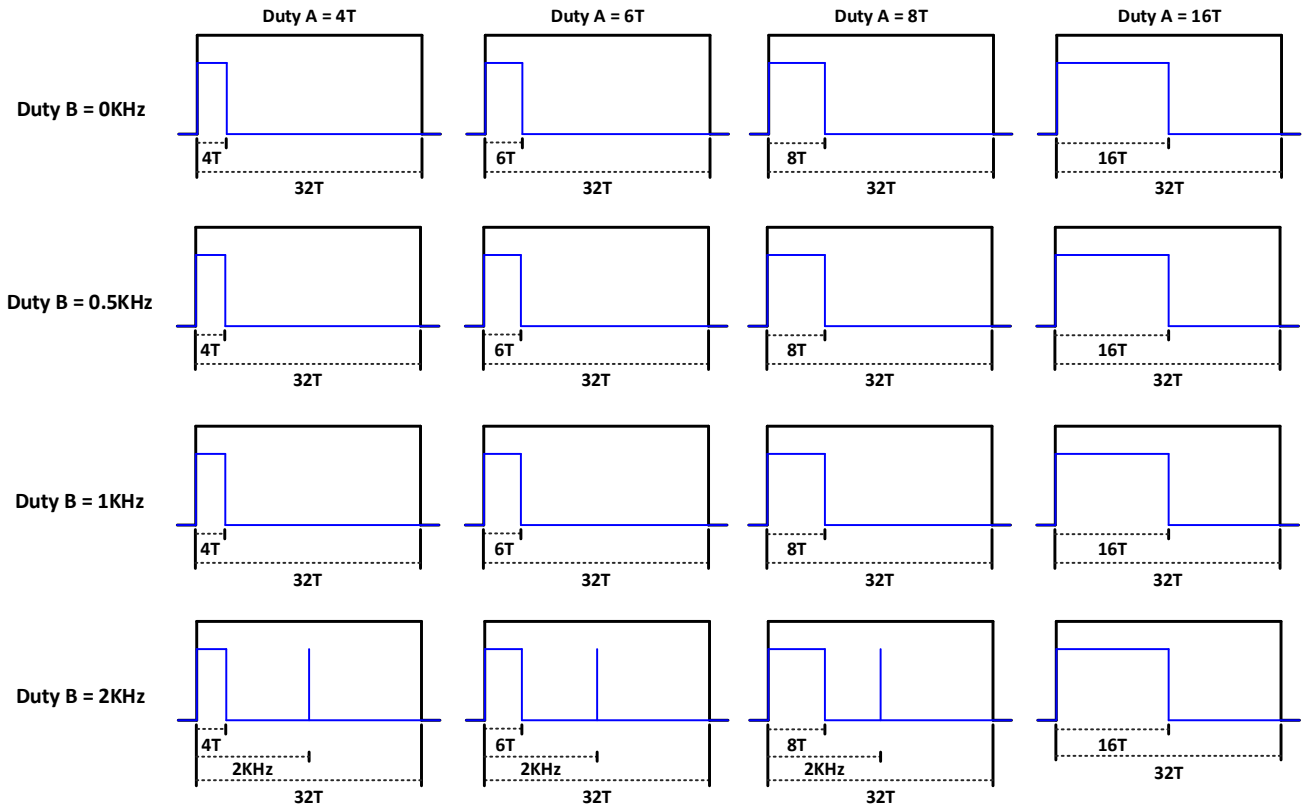
Waveform of DUTYA & DUTYB at LCD clock = 256 Hz



Waveform of DUTYA & DUTYB at LCD clock = 512 Hz



Waveform of DUTYA & DUTYB at LCD clock = 1024 Hz



26.6 LCD Pin Control

LCD driver output 4, 5, 6 or 8-com waveform controlled by LCDMODE[1:0] bit. COM4/ COM5/ COM6/ COM7 share with SEG35/SEG34/SEG33/SEG32.

Register setup			I/O status					
LCDEN	LCDMODE[1:0]	LCDSEGENn	COM0 ~COM3	COM4~COM7 (SEG35~SEG31)				SEG0 ~SEG31
				COM4	COM5	COM6	COM7	
0	X	X	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
1	00 (4-COM)	0	COM	GPIO	GPIO	GPIO	GPIO	GPIO
1	01 (5-COM)	0	COM	COM	GPIO	GPIO	GPIO	GPIO
1	10 (6-COM)	0	COM	COM	COM	GPIO	GPIO	GPIO
1	11 (8-COM)	0	COM	COM	COM	COM	COM	GPIO
1	00 (4-COM)	1	COM	SEG	SEG	SEG	SEG	SEG
1	01 (5-COM)	1	COM	COM	SEG	SEG	SEG	SEG
1	10 (6-COM)	1	COM	COM	COM	SEG	SEG	SEG
1	11 (8-COM)	1	COM	COM	COM	COM	COM	SEG

26.7 SEG Bit Map and RAM Location

User control the SEGn register to display, set a bit of register to turn on a corresponding dot.

Bit map	COM 7	COM 6	COM 5	COM 4	COM 3	COM 2	COM 1	COM 0	
SEG 0	C7ON0	C6ON0	C5ON0	C4ON0	C3ON0	C2ON0	C1ON0	C0ON0	0
SEG 1	C7ON1	C6ON1	C5ON1	C4ON1	C3ON1	C2ON1	C1ON1	C0ON1	1
SEG 2	C7ON2	C6ON2	C5ON2	C4ON2	C3ON2	C2ON2	C1ON2	C0ON2	2
.				.					.
.				.					.
.				.					.
.				.					.
.				.					.
.				.					.
SEG 33	C7ON33	C6ON33	C5ON33	C4ON33	C3ON33	C2ON33	C1ON33	C0ON33	33
SEG 34	C7ON34	C6ON34	C5ON34	C4ON34	C3ON34	C2ON34	C1ON34	C0ON34	34
SEG 35	C7ON35	C6ON35	C5ON35	C4ON35	C3ON35	C2ON35	C1ON35	C0ON35	35
	H	G	F	E	D	C	B	A	

LCD RAM locates in address from 0xF028 to 0xF04B.

LCD RAM location relate to COM0 ~ COM3 vs. SEG0 ~ SEG35 LCD as show in following table.

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
	COM0	**COM1**	**COM2**	**COM3**	**-**	**-**	**-**	**-**
SEG 0	F028H.0	F028H.1	F028H.2	F028H.3	N/A	N/A	N/A	N/A
SEG 1	F029H.0	F029H.1	F029H.2	F029H.3	N/A	N/A	N/A	N/A
SEG 2	F03AH.0	F03AH.1	F03AH.2	F03AH.3	N/A	N/A	N/A	N/A
SEG 3	F03BH.0	F03BH.1	F03BH.2	F03BH.3	N/A	N/A	N/A	N/A
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
SEG 35	F04BH.0	F04BH.1	F4BH.2	F04BH.3	N/A	N/A	N/A	N/A

LCD RAM location relate to COM0 ~ COM4 vs. SEG0 ~ SEG34 LCD as show in following table.

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
	COM0	**COM1**	**COM2**	**COM3**	**COM4**	**-**	**-**	**-**
SEG 0	F028H.0	F028H.1	F028H.2	F028H.3	F028H.4	N/A	N/A	N/A
SEG 1	F029H.0	F029H.1	F029H.2	F029H.3	F029H.4	N/A	N/A	N/A
SEG 2	F03AH.0	F03AH.1	F03AH.2	F03AH.3	F03AH.4	N/A	N/A	N/A
SEG 3	F03BH.0	F03BH.1	F03BH.2	F03BH.3	F03BH.4	N/A	N/A	N/A

-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
SEG 34	F04AH.0	F04AH.1	F4AH.2	F04AH.3	F04AH.4	N/A	N/A	N/A
SEG 35 (COM4)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

LCD RAM location relate to COM0 ~ COM5 vs. SEG0 ~ SEG33 LCD as show in following table.

	Bit0	**Bit1**	**Bit2**	**Bit3**	**Bit4**	**Bit5**	**Bit6**	**Bit7**
	COM0	**COM1**	**COM2**	**COM3**	**COM4**	**COM5**	**-**	**-**
SEG 0	F028H.0	F028H.1	F028H.2	F028H.3	F028H.4	F028H.5	N/A	N/A
SEG 1	F029H.0	F029H.1	F029H.2	F029H.3	F029H.4	F029H.5	N/A	N/A
SEG 2	F03AH.0	F03AH.1	F03AH.2	F03AH.3	F03AH.4	F03AH.5	N/A	N/A
SEG 3	F03BH.0	F03BH.1	F03BH.2	F03BH.3	F03BH.4	F03BH.5	N/A	N/A
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
SEG 33	F049H.0	F049H.1	F49H.2	F049H.3	F049H.4	F049H.5	N/A	N/A
SEG 34 (COM5)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
SEG 35 (COM4)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

LCD RAM location relate to COM0 ~ COM7 vs. SEG0 ~ SEG31 LCD as show in following table.

	Bit0	**Bit1**	**Bit2**	**Bit3**	**Bit4**	**Bit5**	**Bit6**	**Bit7**
	COM0	**COM1**	**COM2**	**COM3**	**COM4**	**COM5**	**COM6**	**COM7**
SEG 0	F028H.0	F028H.1	F028H.2	F028H.3	F028H.4	F028H.5	F028H.6	F028H.7
SEG 1	F029H.0	F029H.1	F029H.2	F029H.3	F029H.4	F029H.5	F029H.6	F029H.7
SEG 2	F03AH.0	F03AH.1	F03AH.2	F03AH.3	F03AH.4	F03AH.5	F03AH.6	F03AH.7
SEG 3	F03BH.0	F03BH.1	F03BH.2	F03BH.3	F03BH.4	F03BH.5	F03BH.6	F03BH.7
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
SEG 31	F047H.0	F047H.1	F47H.2	F047H.3	F047H.4	F047H.5	F047H.6	F047H.7

SEG 32 (COM7)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
SEG 33 (COM6)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
SEG 34 (COM5)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
SEG 35 (COM4)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

26.8 LCD Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDM1	LCDBIAS	LCDMODE1	LCDMODE0	LCDBNK	LCDRATE1	LCDRATE0	-	LCDEN
LCDM2	RCMOD	BGM	DUTY1	DUTY0	VCP3	VCP2	VCP1	VCP0
LCDM3	-	-	-	-	ENLDOBIAS	DUTYB1	DUTYB0	-
LCDSEGEN0	SEG7EN	SEG6EN	SEG5EN	SEG4EN	SEG3EN	SEG2EN	SEG1EN	SEG0EN
LCDSEGEN1	SEG15EN	SEG14EN	SEG13EN	SEG12EN	SEG11EN	SEG10EN	SEG79EN	SEG8EN
LCDSEGEN2	SEG23EN	SEG22EN	SEG21EN	SEG20EN	SEG19EN	SEG18EN	SEG17EN	SEG16EN
LCDSEGEN3	SEG31EN	SEG30EN	SEG29EN	SEG28EN	SEG27EN	SEG26EN	SEG25EN	SEG24EN
LCDSEGEN4	-	-	-	-	SEG35EN	SEG34EN	SEG33EN	SEG32EN
SEG0	C7S0	C6S0	C5S0	C4S0	C3S0	C2S0	C1S0	C0S0
…	…	…	…	…	…	…	…	…
SEG34	C7S34	C6S34	C5S34	C4S34	C3S34	C2S34	C1S34	C0S34

LCDM1 Register (0xF020)

Bit	Field	Type	Initial	Description
7	LCDBIAS	R/W	0	LCD bias mode control bit 0: 1/3 bias 1: 1/4 bias
6..5	LCDMODE[1:0]	R/W	0	LCD driver 4-COM ~ 8-COM control bit 00: 4-COM 01: 5-COM (SEG35 as COM4) 10: 6-COM (SEG35~SEG34 as COM4~COM5) 11: 8-COM (SEG35~SEG32 as COM4~COM7)
4	LCDBNK	R/W	0	LCD blank control bit 0: Normal display 1: All of the LCD dots turn off

3..2	LCDRATE[1:0]	R/W	0	LCD clock rate control bit 00: 256Hz 01: 512Hz 10: 1024Hz 11: Reserved.
1	Reserved	R	0	
0	LCDEN	R/W	0	LCD driver enable bit 0: LCD driver disable 1: LCD driver enable

LCDM2 Register (0xF021)

Bit	Field	Type	Initial	Description
7	RCMOD	R/W	0	RCMOD: LCD mode select 0: C-Type LCD, VLCD Pad is depend on VCP[3:0] 1: R-Type LCD, VLCD Pad is VDD
6	BGM	R/W	1	LCD low power mode control bit 0: Enable low power mode 1: Normal operation mode
5..4	DUTYA[1..0]	R/W	00	LCD pump output driving capacity control bits* 00: 4T, 01: 6T 10: 8T, 11: 16T
3..0	VCP[3:0]	R/W	0100	Only support C-Type LCD, VLCD output voltage control bits 0000: 2.6V, 0001 : 2.7V 0010: 2.8V, 0011 : 2.9V 0100: 3.0V, 0101 : 3.1V 0110: 3.2V, 0111 : 3.3V 1000: 3.4V, 1001 : 3.5V 1010: 3.6V, 1011 : 3.7V 1100: 3.9V, 1101 : 4.1V 1110: 4.3V, 1111 : 4.5V

* DUTYA [1:0] is controllable when BGM=0, which is set for LCD low power consumption. Recommend use 16T Duty for display quality. T = 1 / (ILRC or L'XTAL).

LCDM3 Register (0xF022)

Bit	Field	Type	Initial	Description
3	ENLDOBIAS	R/W	0	LCD low power + mode control bit. 0: Disable low power + mode.

				1: Enable low power + mode.
2..1	DUTYB[1:0]	R/W	00	LCD low power duty b Pulse control bits. * 00: Disable, 10: 1kHz 01: 0.5kHz, 11: 2kHz
Else	Reserved	R/W	0	

* DUTYB [1:0] is controllable when BGM=0, which is set for LCD low power consumption. Recommend use 2kHz for display quality.

LCDSEGEN0 Register (0xF023)

Bit	Field	Type	Initial	Description
7..0	SEGnEN[7:0]	R/W	0x00	LCD SEGn channel control bit. 0: GPIO pin. 1: SEG pin.

LCDSEGEN1 Register (0xF024)

Bit	Field	Type	Initial	Description
7..0	SEGnEN[15:8]	R/W	0x00	LCD SEGn channel control bit. 0: GPIO pin. 1: SEG pin.

LCDSEGEN2 Register (0xF025)

Bit	Field	Type	Initial	Description
7..0	SEGnEN[23:16]	R/W	0x00	LCD SEGn channel control bit. 0: GPIO pin. 1: SEG pin.

LCDSEGEN3 Register (0xF026)

Bit	Field	Type	Initial	Description
7..0	SEGnEN[31:24]	R/W	0x00	LCD SEGn channel control bit. 0: GPIO pin. 1: SEG pin.

LCDSEGEN4 Register (0xF027)

Bit	Field	Type	Initial	Description
7..4	Reserved	R	0x00	
3..0	SEGnEN[35:32]	R/W	0x00	LCD SEGn channel control bit. 0: GPIO pin. 1: SEG pin.

SEGn Register (SEG0: 0xF028 ~ SEG34: 0xF04B)

Bit	Field	Type	Initial	Description
7..0	CmSn [7:0]	R/W	0x00	LCD SEGn data buffer*.

* m= 0~7, n = 0 ~ 34.

27 CRC

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from 8-bit data word and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. The CRC calculation circuit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

The CRC generator keeps running in IDLE mode but doesn't have wake-up function. In stop mode, the CRC generator is stop.

- Support
  CRC-16 polynomial: $X^{16}+X^{15}+X^{2}+1$
  CRC-16-CCITT polynomial: $X^{16}+X^{12}+X^{5}+1$
- Handles 8-bit data size
- Single input/output 8-bit data register
- Input buffer to avoid bus stall during calculation
- 64KB ROM calculating time is 4ms.

27.1 CRC Calculation Procedure

The CRC generator supports 2 calculation modes to obtain CRC code including ROM auto-calculation mode and data calculation mode.

ROM auto-calculation mode procedure:

- Support select CRC execute range by CRCROM[1:0] bits.
  If INFBLK bit = 0, CRC executes main block
  If CRCROM[1:0] = 00, the CRC executes range is IROM 0x0000~0x3FFF.
  If CRCROM[1:0] = 01, the CRC executes range is IROM 0x0000~0x7FFF.
  If CRCROM[1:0] = 10, the CRC executes range is IROM 0x0000~0xF7FF.
  If CRCROM[1:0] = 11, the CRC executes range is IROM 0x0000~0xFFFF.
  If INFBLK bit = 1, CRC executes information block
  If CRCROM[1:0] = 00, the CRC executes range is IBROM 0x0000~0x0FFF (boot loader area).
  If CRCROM[1:0] = 01, the CRC executes range is IBROM 0x1000~0x11FF (data flash area).
  If CRCROM[1:0] = Others, reserved.
- Select CRC polynomial by CRCPOL bit. When CRCPOL=0, CRC-16-CCITT ($X^{16}+X^{12}+X^{5}+1$) is selected. Otherwise, the CRC-16($X^{16}+X^{15}+X^{2}+1$) is selected.
- Set CRCRST bit to reset initial seed value/ CRC data buffer and BUSY bit to 0.
- Set URCRCEN bit to start CRC calculation and check BUSY bit.

- CRC calculation is finished until BUSY bit from 1 to 0. Read CRC code from CRCDATH/L.

Data calculation mode procedure:

- Select CRC polynomial by CRCPOL bit. When CRCPOL=0, CRC-16-CCITT (X16+X12+X5+1) is selected. Otherwise, the CRC-16(X^{16}+X^{15}+X^2+1) is selected.
- Set CRCRST bit to reset initial seed value/ CRC result and BUSY bit to 0.
- Key in data to CRCDATL.
- Set URCRCEN bit to start CRC calculation and check BUSY bit.
- CRC calculation is finished until BUSY bit from 1 to 0. Read CRC code from CRCDATH/L

27.2 CRC Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCM	URCRCEN	BUSY	CRCRST	CRCPOL	CRCROM1	CRCROM0	-	CRCEN
CRCDATL	CRCDAT7	CRCDAT6	CRCDAT5	CRCDAT4	CRCDAT3	CRCDAT2	CRCDAT1	CRCDAT0
CRCDATH	CRCDAT15	CRCDAT14	CRCDAT13	CRCDAT12	CRCDAT11	CRCDAT10	CRCDAT9	CRCDAT8

CRCM Register (0xF1)

Bit	Field	Type	Initial	Description
7	URCRCEN	R/W	0	Enable bit of the CRC calculation User ROM. 0: Disable 1: Enable
6	BUSY	R/W	0	Disable. Stop/Finish operation 0: CRC calculation finished. 1: CRC calculation is in process.
5	CRCRST	R/W	0	Reset bit. 0: No effect. 1: Reset the CRC calculation circuit.
4	CRCPOL	R/W	0	CRC Polynomial 0: CRC-16-CCITT 1: CRC-16
3..2	CRCROM [1:0]	R/W	0x00	CRC EEPROM calculation range. 00: 0x0000~0x3FFF (1/4 ROM). 01: 0x0000~0x7FFF (1/2 ROM). 10: 0x0000~0xF7FF (Reserve last 4 page) 11:0x0000~0xFFFF (Full ROM)

0	CRCEN	R/W	0	Enable bit of the CRC IP 0: Disable. 1: Enable.

CRCDATL Register (0xF2)

Bit	Field	Type	Initial	Description
7..0	CRCDAT[7:0]	R/W	0x00	Low byte of 16-bit CRC data.

CRCDATH Register (0xF3)

Bit	Field	Type	Initial	Description
7..0	CRCDAT[15:8]	R/W	0x00	High byte of 16-bit CRC data.

28 In-System Program

The SN8F5869 MCU integrated device feature in-system programmable (ISP) FLASH memory for convenient, upgradeable code storage. The FLASH memory may be programmed via the SONiX 8051 MCU programming interface or by application code. The SN8F5869 provides security options at the disposal of the designer to prevent unauthorized access to information stored in FLASH memory. ISP Flash ROM provided user an easy way to storage data into Flash ROM. The ISP concept is memory mapping idea that is to move RAM buffer to flash ROM. Choice ROM/RAM address and executing ROM programming command – PECMD, after programming words which controlled by PERAMCNT, PERAML/PERAMCNT data will be programmed into address PEROML/PEROMH.

	RAM (byte)			Flash ROM (byte)
RAM Address	bit7 ~ bit0		ROM Address	bit7 ~ bit0
X	DATA0		Y	DATA0
X+1	DATA1		Y+1	DATA1
X+2	DATA2	=>	Y+2	
X+3	DATA3		Y+3	
…			…	
…			…	
X+N	DATAN		Y+M	DATAN

During Flash program or erase operation, the MCU is stalled, although peripherals (Timers, WDT, I/O, PWM, etc.) remain active. When PECMD register is set to execute ISP program and erase operations, the program counter stops, op-code can't be dumped from flash ROM, instruction stops operating, and program execution is hold not to active. At this time hardware depends on ISP operation configuration to do flash ROM erasing and flash ROM programming automatically. After ISP operation is finished, hardware releases system clock to make program counter running, system returns to last operating mode, and the next instruction is executed. Recommend to add two "NOP" instructions after ISP operations.

- ISP flash ROM erase time = 4ms……1-page, 512-byte.
- ISP flash ROM program time = 120us……1- byte.
  …
  ISP flash ROM program time = 1390us……128- byte.

28.1 Erase

ISP flash ROM erase operation is to clear flash ROM contents to blank status "1". Erasing ROM length is 512-byte and has ROM page limitation. ISP flash ROM erase ROM map is as following:

ISP ROM MAP		ROM address bit0~bit8 (hex) =0
IROM address bit9~bit15 (hex)	0000	These pages include reset vector and interrupt sector. We strongly recommend to reserve the area not to do ISP erase.
	0200	One ISP Erase Page
	0400	One ISP Erase Page
	…	One ISP Erase Page
	7000	One ISP Erase Page
	7200	One ISP Erase Page
	…	One ISP Erase Page
	FC00	One ISP Erase Page
	FE00	One ISP Erase Page
IBROM address bit9~bit15 (hex)	0000	These pages include boot loader area. We strongly recommend to reserve the area not to do ISP erase.
	…	
	0E00	
	1000	One ISP Erase Page
	1200	These pages include ROM reserved area. We strongly recommend to reserve the area not to do ISP erase.
	…	
	1E00	

ISP flash ROM erase density is 512- byte which limits erase page boundary. The first 256- byte of flash ROM (0x0000~0x00FF) includes reset vector and interrupt vectors related essential program operation, we strongly recommend do not execute ISP flash ROM erase operation in this page. Flash ROM area 0x0200~0xFFFF includes 127-page for ISP flash ROM erase operation.

The first step to do ISP flash ROM erase is to address ROM-page location. The address must be the head location of a page area, e.g. 0x0200, 0x0400…0x7000, 0x7200 and 0xFE00. PEROML [7:0] and PEROMH [7:0] define the target starting address [15:0] of flash ROM. Write the start address into PEROML and PEROMH registers, set PECMD register to “0xC3”, and the system start to execute ISP flash ROM erase operation.

Except Main code ISP (0x0200~0xFFFF) 127-page. SN8F5869 build-up Data flash memory (0x1000~0x11FF) 1-page in IBROM. Before erasing data flash memory, the INFBLK bit must be set. After that, data flash memory erase function is the same with main code.

28.2 Page Program

ISP flash ROM program operation is to write data into flash ROM by program. Program ROM doesn't limit written ROM address and length, but limits 128- byte density of one page. The number of ISP flash ROM program operation can be 1- byte ~ 128- byte at one time, but these words must be in the same page. ISP flash ROM program ROM map is as following:

ISP ROM MAP		ROM address bit0~bit6 (hex) =0
IROM address bit7~bit15 (hex)	0000	These pages include reset vector and interrupt sector. We strongly recommend to reserve the area not to do ISP.
	0080	
	0100	
	0180	
	0200	One ISP Program Page
	0280	One ISP Program Page
	…	One ISP Program Page
	7000	One ISP Program Page
	7080	One ISP Program Page
	…	One ISP Program Page
	FF00	One ISP Program Page
	FF80	One ISP Program Page
IBROM address bit7~bit15 (hex)	0000	These pages include boot loader area. We strongly recommend to reserve the area not to do ISP.
	…	
	0F80	
	1000	One ISP Program Page
	1080	One ISP Program Page
	1100	One ISP Program Page
	1180	One ISP Program Page
	1200	These pages include ROM reserved area. We strongly recommend to reserve the area not to do ISP.
	…	
	1E80	

ISP flash ROM program page density is 128- byte which limits program page boundary. The first 256-byte of flash ROM (0x0000~0x00FF) includes reset vector and interrupt vectors related essential program operation, we strongly recommend do not execute ISP flash ROM program operation in this page. Flash ROM area 0x0100~0xFFFF includes 510-page for ISP flash ROM program operation.

ISP flash ROM program operation is a simple memory mapping operation. The first step is to plan a RAM area to store programmed data and keeps the RAM address for ISP RAM addressing. The second step is to plan a ROM area will be programmed from RAM area in ISP flash ROM program operation. The RAM addressing is through PERAML [7:0] 8-bit buffer to configure the start RAM

address.

ISP programming length is 1- byte ~128- byte. ISP flash ROM programming length is controlled by PERAMCNT [6:0] bits which is 7-bit format. Before ISP ROM programming execution, set the length by program. PEROML [7:0] and PEROMH [7:0] define the target starting address [15:0] of flash ROM. Write the start address into PEROML and PEROMH registers, set PECMD register to “0xC3” and the system start to execute ISP flash ROM erase operation, set PECMD register to “0x5A” and the system start to execute ISP flash ROM program operation. If the programming length is over ISP flash ROM program page boundary, the hardware immediately stops programming flash ROM after finishing programming the last word of the ROM page. So it is very important to plan right ROM address and programming length.

These configurations must be setup completely before starting Page erase and program. ISP is configured using the following steps:

1. Save program data into IRAM. The data continues for 128 bytes.
2. Set the start address of the content location to PERAM.
3. Set the start address of the anticipated update area to PEROM [15:0]. (By PEROMH/PRROML/ PEROMHH registers)
4. Set the ISP programming length of PERAMCNT.
5. Write ‘0xC3’ into PECMD [7:0] to page erase (512 bytes/page).
6. Write ‘0x5A’ into PECMD [7:0] to page program (max 128 bytes/page).
7. Write ‘NOP’ instruction twice.
8. Must Write PEROMHH Bit2 = 0, after Data memory program process.

As an example, assume the program memory (IROM, 0xFE00 – 0xFFFF) is the anticipated update area; the content is already stored in IRAM address 0x40 – 0xBF. To perform the in-system program, simply write starting IROM address 0xFE00 to PROMH/PROML registers, and then specify buffer starting address 0x40 to EPRAM register. Set the ISP programming length of PERAMCNT. Subsequently, write ‘0xC3’ into PECMD [7:0] registers and then write ‘0x5A’ into PECMD [7:0] registers to duplicate the buffer’s data to IROM.

✷ ***Note:***

1. Watch dog timer should be clear before the Flash write (program) operation, or watchdog timer would overflow and reset system during ISP operating.

2. Don’t execute ISP flash ROM program operation for the first page, or affect program operation.

3. ISP operation (page program) actually perform Flash erase and program procedures in the background. Don't execute ISP flash ROM program operation in low-voltage condition (ex. VDD < 2.5V), or ISP operation maybe not complete before power-off.

28.3 In-system Program Register

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PERAM	PERAM7	PERAM6	PERAM5	PERAM4	PERAM3	PERAM2	PERAM1	PERAM0
PEROMH	PEROM15	PEROM14	PEROM13	PEROM12	PEROM11	PEROM10	PEROM9	PEROM8
PEROML	PEROM7	PEROM6	PEROM5	PEROM4	PEROM3	PEROM2	PEROM1	PEROM0
PECMD	PECMD7	PECMD6	PECMD5	PECMD4	PECMD3	PECMD2	PECMD1	PECMD0
PERAMCNT	-	PRRAM6	PRRAM5	PRRAM4	PRRAM3	PRRAM2	PRRAM1	PRRAM0
PEROMHH	-	-	-	-	-	INFBLK	-	-

PEROMHH Register (0xBF)

Bit	Field	Type	Initial	Description
2	INFBLK	R/W	0	Main Block / Information Block select switch 0: Main Block 1: Information Block
Else	Reserved	R/W	0	

PERAM Register (0xBD)

Bit	Field	Type	Initial	Description
7..0	PERAM[7:0]	R/W	0x00	The first address of data buffer (IRAM)

PEROMH Register (0xBC)

Bit	Field	Type	Initial	Description
7..0	PEROM[15:8]	R/W	0x00	The first address (15^{th}– 8^{th} bit) of program page (IROM)

PEROML Register (0xBB)

Bit	Field	Type	Initial	Description
7..0	PEROM[7:0]	R/W	000	The first address (7^{th}– 0^{th} bit) of program page (IROM)

PECMD Register (0xBA)

Bit	Field	Type	Initial	Description

7..0	PECMD[7:0]	W	-	0x5A: Start page program procedure (128 bytes/page) 0xC3: Start page erase (512 bytes/page) Else values: Reserved*(1)

*(1) Not permitted to write any other to PECMD register.

PERAMCNT Register (0xBE)

Bit	Field	Type	Initial	Description
7	Reserved	R	00	
6..0	PERAM[6:0]	R/W	0x00	Defines the number of byte wanted to be programmed 0000000: ISP programming length is 1 -byte. 0000001: ISP programming length is 2 -byte. … 1111110: ISP programming length is 127 -byte. 1111111: ISP programming length is 128 -byte.

29 Clock Fine-Tuning

SN8F5869 builds in clock fine-tuning function that is a procedure to fine-tune system clock frequency by firmware. The function is enabled by code option (CK_Fine_Tuning). When CK_Fine_Tuning = 0, the clock fine-tuning function is disabled. When CK_Fine_Tuning = 1, the clock fine-tuning function is enabled. After system power-on, the 10-bit initial clock trim value will be loaded to FRQ[9:0] buffer by hardware. The trim value corresponds to IHRC 32MHz. Change the trim value of FRQ[9:0] to modify internal clock frequency.

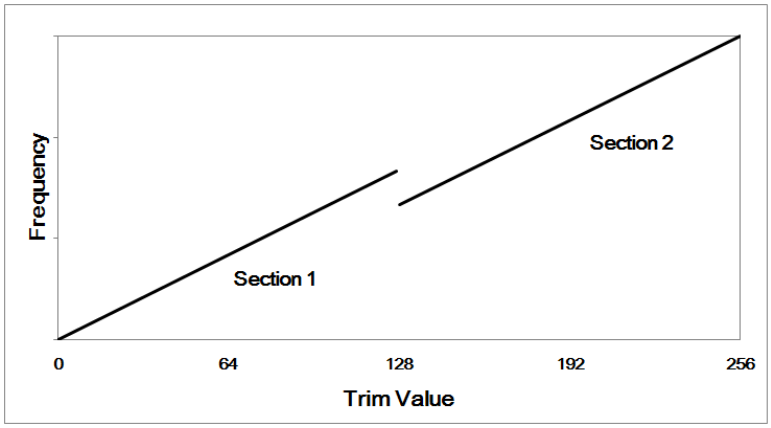
29.1 Clock Trim Section

Clock fine-tuning consists of 8 trim sections as Table 29-1. Each section includes 128 trim steps and each step is about (32MHz *0.1%) in the same section. The larger the Trim value, the faster the frequency.

Table 29-1 Clock Trim Section

Section	Trim Value	Frequency
1	000H ~ 07FH	Low
2	080H ~ 0FFH	
3	100H ~ 17FH	
4	180H ~ 1FFH	
5	200H ~ 27FH	
6	280H ~ 2FFH	
7	300H ~ 37FH	
8	380H ~ 3FFH	High

Each adjacent section has a frequency gap as below. Thus the frequency in trim value =127 will faster than trim value =128.



29.2 Clock Fine-Tuning Procedure

Theses configurations must be setup completely before starting clock fine-tuning. The steps as the following:

1. Select code option CK_Fine_Tuning = 1 to enable clock fine-tuning function.
2. As the Max. IROM fetching cycle is 24MHz.
3. Read 10-bit 32MHz trim value from FRQ[9:0]
4. Check the fine-tuning range from the Table 29-1.
5. Write the new clock trim value to FRQ[9:0].
6. Write ‘0x3C’ into FRQCMD [7:0] to trigger clock fine-tuning function.

✷ ***Note: Please check IROM fetching cycle ≦ 24MHz to avoid system error.***

29.3 Clock Fine-Tuning Register

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRQH	-	-	-	-	-	-	FRQ9	FRQ8
FRQL	FRQ7	FRQ6	FRQ5	FRQ4	FRQ3	FRQ2	FRQ1	FRQ0
FRQCMD	FRQCMD7	FRQCMD6	FRQCMD5	FRQCMD4	FRQCMD3	FRQCMD2	FRQCMD1	FRQCMD0

FRQ Register (FRQH:0xAB, FRQL:0xAA)

Bit	Field	Type	Initial	Description
9..0	FRQ[9:0]	R/W	0x00	The system clock calibration value

FRQCMD Register (0xAC)

Bit	Field	Type	Initial	Description
7..0	FRQCMD[7:0]	W	0x00	0x3C: Start clock fine-tuning procedure Else values: Reserved*(1)

*(1) Not permitted to write any other to FRQCMD register.

30 ILRC Auto-Calibration

30.1 Auto-Calibration Operation

ILRC auto-calibration function is hardware calibration to support 16KHz ILRC. The calibration function is enabled by CALEN bit. After setup CALEN bit, the system starts to calibrate ILRC frequency to 16KHz. Calibration time is about 20ms. The CALEN bit is reset to logic 0 when the calibration is complete. After the calibration is complete, the circuit will set CALDONE bit if ILRC calibration success.

If user want to manually adjust the ILRC frequency, the method is that writes you want trim value to LFRQ[8:0], and then writes 0xB4 to FRQCMD. The LFRQ[8:0] trim value will be loaded into ILRC IP.

30.2 Clock Fine-Tuning Register

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LFRQH	-	-	-	-	-	-	-	LFRQ8
LFRQL	LFRQ7	LFRQ6	LFRQ5	LFRQ4	LFRQ3	LFRQ2	LFRQ1	LFRQ0
FRQCMD	FRQCMD7	FRQCMD6	FRQCMD5	FRQCMD4	FRQCMD3	FRQCMD2	FRQCMD1	FRQCMD0
CLKCAL	CALEN	CALDONE	-	-	-	-	-	-

LFRQ Register (LFRQH:0xAE, LFRQL:0xAD)

Bit	Field	Type	Initial	Description
15..9	Reserved	R	0x00	
8..0	LFRQ[8:0]	R/W	0x00	The system ILRC calibration value

FRQCMD Register (0xAC)

Bit	Field	Type	Initial	Description
7..0	FRQCMD[7:0]	W	0x00	0x4B: Start ILRC calibration procedure 0xB4: ILRC trim value loaded into ILRC IP Else values: Reserved

CLKCAL Register (0xAF)

Bit	Field	Type	Initial	Description
7	CALEN	R/W	0	ILRC calibration enable bit 0: Disable 1: Enable (automatically cleared by the end of calibration)
6	CALDONE	R/W	0	ILRC calibration result

				0: Calibration fail. 1: Calibration pass, ILRC frequency is 16KHz
5..0	Reserved	R	0x00	

31 Single Wire Asynchronous Interface (SWAT)

SWAT function is a single wire transmission interface for system debug mode.

- Support single-wire debug interface.
- Direct debug access to all memories, registers and peripherals.

31.1 Debug Mode

System debug mode is default enabled. When system power on, SWAT function is enabled and P0.7 acts as SWAT pin for debug interface. User can disable SWAT function by DEGCMD register in order to use P0.7 as GPIO. When DEGCMD= 0x00, SWAT function is disabled and P0.7 acts as GPIO. User can set DEGCMD= 0xA5 to enable SWAT function again. SWAT function can't active under idle/ stop mode. User code must disable SWAT function before system enters idle/ stop mode.

31.2 Internal Pull-Up Resistors on SWAT pin

To avoid any uncontrolled IO levels, the device embeds internal pull-up resistor on SWAT input pin. Once a SWAT function is disabled by DEGCMD register, the GPIO controller takes control again.

31.3 SWAT Register

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEGCMD	DEGCMD7	DEGCMD6	DEGCMD5	DEGCMD4	DEGCMD3	DEGCMD2	DEGCMD1	DEGCMD0

DEGCMD Register (0xC1)

Bit	Field	Type	Initial	Description
7..0	DEGCMD[7:0]	R/W	0xA5	SWAT pin control 0xA5: Enable SWAT pin. (P0.7 acts as SWAT pin and internal pull-up is enabled) 0x00: Disable SWAT pin. (P0.7 acts as GPIO pin and internal pull-up is disabled) Else values: Reserved*(1)

*(1) Not permitted to write any other to DEGCMD register.

32 Electrical Characteristics

32.1 Absolute Maximum Ratings

Voltage applied at VDD to VSS ..... - 0.3V to 6.0V
Voltage applied at any pin to VSS..... - 0.3V to VDD+0.3V
Operating ambient temperature..... -40°C to 105°C
Storage ambient temperature ..... -40°C to 125°C

32.2 System Operation Characteristics

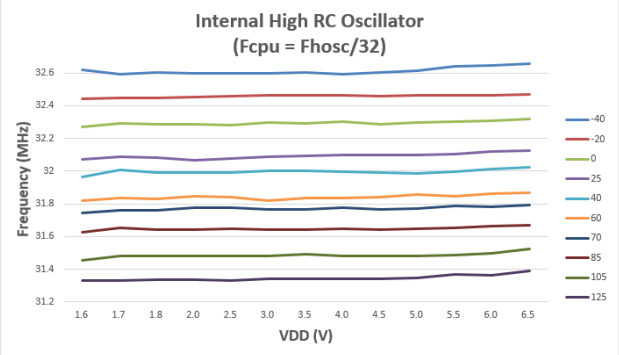
	Parameter	Test Condition	Min	TYP	MAX	UNIT
VDD	Operating voltage	Fcpu = 1MHz	1.8		5.5	V
V_{DR}	RAM data retention Voltage		0.55			V
V_{POR}	VDD rising rate*		0.05			V/ms
I_{DD1}	Normal mode supply current (32MHz IHRC)	VDD = 3V, Fcpu = 1MHz		0.90		mA
		VDD = 5V, Fcpu = 1MHz		0.95		mA
		VDD = 3V, Fcpu = 4MHz		1.20		mA
		VDD = 5V, Fcpu = 4MHz		1.25		mA
		VDD = 3V, Fcpu = 16MHz		1.65		mA
		VDD = 5V, Fcpu = 16MHz		1.70		mA
	Normal mode supply current (24MHz Crystal)	VDD = 3V, Fcpu = 24MHz		2.90		mA
		VDD = 5V, Fcpu = 24MHz		4.30		mA
	Normal mode supply current (16MHz Crystal)	VDD = 3V, Fcpu = 1MHz		1.20		mA
		VDD = 5V, Fcpu = 1MHz		2.40		mA
		VDD = 3V, Fcpu = 4MHz		1.60		mA
		VDD = 5V, Fcpu = 4MHz		2.70		mA
		VDD = 3V, Fcpu = 16MHz		2.10		mA
		VDD = 5V, Fcpu = 16MHz		3.20		mA
	Normal mode supply current (4MHz Crystal)	VDD = 3V, Fcpu = 1MHz		0.75		mA
		VDD = 5V, Fcpu = 1MHz		1.50		mA
		VDD = 3V, Fcpu = 4MHz		1.10		mA
		VDD = 5V, Fcpu = 4MHz		1.80		mA
I_{DD2}	STOP mode supply current	VDD = 3V		1.2	4.0	µA
		VDD = 5V		1.2	4.0	µA
I_{DD3}	STOP mode supply current (ILRC enable STWK=1)	VDD = 5V		2.7		µA
I_{DD5}	IDLE mode supply current	VDD = 3V, 32MHz IHRC		0.65		mA

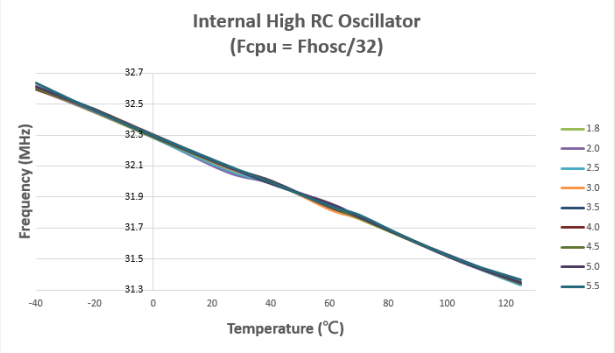
	(Fcpu = 1MHz)	VDD = 5V, 32MHz IHRC		0.70		mA
		VDD = 3V, 24MHz Crystal		1.25		mA
		VDD = 5V, 24MHz Crystal		2.70		mA
		VDD = 3V, 16MHz Crystal		0.95		mA
		VDD = 5V, 16MHz Crystal		2.05		mA
		VDD = 3V, 4MHz Crystal		0.50		mA
		VDD = 5V, 4MHz Crystal		1.20		mA
F_{IHRC}	Internal high clock generator	VDD = 1.8V to 5.5V, 25°C	-0.5%	32	+0.5%	MHz
		VDD = 1.8V to 5.5V, -40°C to 105°C	-2.0%	32	+2.0%	MHz
F_{ILRC}	Internal low clock generator*	VDD = 1.8V to 5.5V, 25°C Non-trimmed	-50%	16	+50%	KHz
		VDD = 1.8V to 5.5V, 25°C Trimmed in normal mode	-1.0%	16	+1.0%	KHz
		VDD = 1.8V to 5.5V, 25°C Trimmed in STOP mode	-2.0%	16	+2.0%	KHz
V_{LVD}	LVD detect voltage	25°C	1.6	1.7	1.8	V
			1.9	2.0	2.1	V
			2.1	2.2	2.3	V
			2.3	2.4	2.5	V
			2.6	2.7	2.8	V
			2.9	3.0	3.1	V
			3.2	3.3	3.4	V
			3.5	3.6	3.7	V
V_{ESD_HBM}	ESD human body mode		4000			V
V_{ESD_CDM}	ESD charged device model		750			V

* Parameter(s) with star mark are non-verified design reference. Ambient temperature is 25°C.

- IHRC Frequency - Temperature Graph

  The IHRC Graphs are for design guidance, not tested or guaranteed. In some graphs, the data presented are outside specified operating range. This is for information only and devices are guaranteed to operate properly only within the specified range.





32.3 GPIO Characteristics

	Parameter	Test Condition	Min	TYP	MAX	UNIT
V_{IL}	Low-level input voltage		VSS		0.3VDD	V
V_{IH}	High-level input voltage		0.7VDD		VDD	V
I_{LEKG}	I/O port input leakage current	V_{IN} = VDD			2	µA
R_{UP}	Pull-up resister	VDD = 3V	80	100	120	kΩ
		VDD = 5V	48	60	72	kΩ
R_{DN}	Pull-down resister	VDD = 3V	80	100	120	kΩ
		VDD = 5V	48	60	72	kΩ
I_{OH1}	I/O output source current High current in PDRV =0	VDD = 5V, V_O = VDD-0.5V	8	15		mA
I_{OH2}	I/O output source current Low current in PDRV =1	VDD = 5V, V_O = VDD-0.5V	15	30		mA
I_{OH3}	I/O output source current Low current in PDRV =1 (LXIN/LXOUT)	VDD = 5V, V_O = VDD-0.5V	8	15		mA
I_{OL1}	I/O sink current High current in PDRV =0	VDD = 5V, V_O = VSS+0.5V	8	15		mA
I_{OL2}	I/O sink current Low current in PDRV =1	VDD = 5V, V_O = VSS+0.5V	15	30		mA

* Ambient temperature is 25°C.

32.4 ADC Characteristics

	Parameter	Test Condition	Min	TYP	MAX	UNIT
V_{ADC}	Operating voltage		2.0		5.5	V
V_{AIN}	AIN channels input voltage	VDD = 5V	0		V_{REFH}	V
V_{REFH}	AVREFH pin input voltage	VDD = 5V	2.0		VDD	V
V_{IREF}	Internal VDD reference voltage	VDD = 5V		VDD		V
	Internal 4.5V reference voltage	VDD = 5V	-1%	4.5	+1%	V
	Internal 3V reference voltage	VDD = 5V	-1%	3	+1%	V
	Internal 2V reference voltage	VDD = 5V	-1%	2	+1%	V
	Internal 1.5V reference voltage	VDD = 5V	-1%	1.5	+1%	V
I_{AD}	ADC current consumption	VDD = 3V		0.45		mA
		VDD = 5V		0.50		mA
f_{ADCLK}	ADC clock	VDD = 5V			16	MHz
f_{ADSMP}	ADC sampling rate	VDD = 5V			1	MHz
t_{ADEN}	ADC function enable period	VDD = 5V	100			µs
DNL	Differential nonlinearity*	f_{ADSMP} = 250kHz		±1.5		LSB
		f_{ADSMP} = 1MHz		±2		LSB
INL	Integral Nonlinearity*	f_{ADSMP} = 250kHz		±2		LSB
		f_{ADSMP} = 1MHz		±2.5		LSB
NMC	No missing code*	f_{ADSMP} = 250kHz	10	11	12	Bit
V_{OFFSET}	Input offset voltage	Non-trimmed	-2	0	2	mV

* Parameters with star mark: VDD = 5V, V_{REFH} = 2.4V, 25°C.

32.5 LCD Characteristics

	Parameter	Test Condition	MIN	TYP	MAX	UNIT
I_{CLCD}	C-Type LCD Low Power Mode Operation Current	VDD = 2.2~ 5V, No panel, Low Power Mode(BGM=0, DUTYA[1:0]=00)		*9		uA
		VDD = 2.2~ 5V, No panel, Low Power Mode(BGM=0, DUTYA[1:0]=01)		*10		uA
		VDD = 2.2~ 5V, No panel, Low Power Mode(BGM=0, DUTYA[1:0]=10)		*11		uA
		VDD = 2.2~ 5V, No panel, Low Power Mode(BGM=0, DUTYA[1:0]=11)		*13		uA
	C-Type LCD Normal Mode Operation Current	VDD = 2.2~ 5V, No panel, Normal Mode(BGM=1, DUTYA[1:0]=xx)		*120		uA
I_{RLCD}	R-Type LCD Low Power Mode Operation Current	VDD = 2.2~ 5V, No panel, Low Power Mode(BGM=0, DUTYA[1:0]=00)		*6.5		uA
		VDD = 2.2~ 5V, No panel, Low Power Mode(BGM=0, DUTYA[1:0]=01)		*7		uA
		VDD = 2.2~ 5V, No panel, Low Power Mode(BGM=0, DUTYA[1:0]=10)		*8		uA
		VDD = 2.2~ 5V, No panel, Low Power Mode (BGM=0, DUTYA[1:0]=11)		*11		uA
	R-Type LCD Normal Mode Operation Current	VDD = 3V, No panel, Normal Mode(BGM=1, DUTYA[1:0]=xx)		*40		uA
		VDD = 5V, No panel, Normal Mode(BGM=1, DUTYA[1:0]=xx)		*50		uA
V_{LCD}	VLCD set 3.0V (VCP [3:0]=0100)	VDD = 2.2~ 5V	2.9	3.0	3.1	V

*Parameter(s) with star mark are non-verified design reference. Ambient temperature is 25°C.

32.6 Flash Memory Characteristics

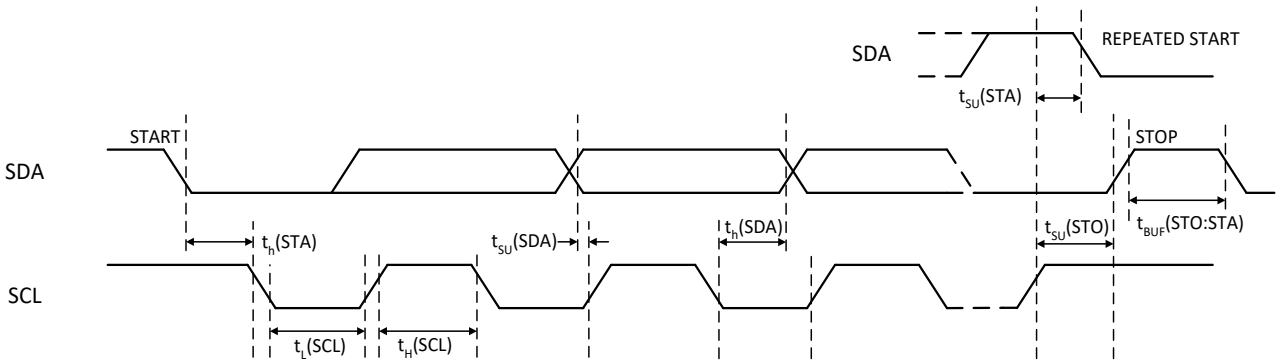
	Parameter	Test Condition	Min	TYP	MAX	UNIT
V_{dd}	Supply voltage		1.8		5.5	V
T_{pen}	Page Endurance time	25°C		*100K		cycle
I_{wrt}	Write current	25°C		3	4	mA
T_{wrt}	Write time	Write 128 bytes, 25°C		1	2	ms

* Parameters with star mark are non-verified design reference.

32.7 I2C interface characteristics

Symbol	Parameter	Typical Formula	UNIT
t_H(SCL)	SCL clock high time	2* fsck	µs
t_L(SCL)	SCL clock low time	2* fsck	µs
t_{SU}(SDA)	SDA setup time	2* fsck -7*Fhosc	µs
t_h(SDA)	SDA data hold time	7*Fhosc	µs
t_h(STA)	START condition hold time	4* fsck	µs
t_{SU}(STA)	Repeated START condition setup time	2* fsck	µs
t_{SU}(STO)	STOP condition setup time	4* fsck +8*Fhosc	µs
T_{BUF}(STO:STA)	STOP to START condition time	4/3* fsck +10*Fhosc	µs

*Standard mode I2C fsck = 100KHz, Fast mode I2C fsck = 400KHz, fhosc=32MHz



33 Instruction Set

This chapter categorizes the SN8F5869 microcontroller's comprehensive assembly instructions. It includes five categories—arithmetic operation, logic operation, data transfer operation, Boolean manipulation, and program branch—which are fully compatible with standard 8051.

Symbol description

Symbol	Description
Rn	Working register R0 - R7
direct	One of 128 internal RAM locations or any Special Function Register
@Ri	Indirect internal or external RAM location addressed by register R0 or R1
#data	8-bit constant (immediate operand)
#data16	16-bit constant (immediate operand)
bit	One of 128 software flags located in internal RAM, or any flag of bit-addressable Special Function Registers
addr16	Destination address for LCALL or LJMP, can be anywhere within the 64-Kbyte page of program memory address space
addr11	Destination address for ACALL or AJMP, within the same 2-Kbyte page of program memory as the first byte of the following instruction
rel	SJMP and all conditional jumps include an 8-bit offset byte. Its range is +127/-128 bytes relative to the first byte of the following instruction
A	Accumulator

Arithmetic operations

Mnemonic	Description
ADD A, Rn	Add register to accumulator
ADD A, direct	Add directly addressed data to accumulator
ADD A, @Ri	Add indirectly addressed data to accumulator
ADD A, #data	Add immediate data to accumulator
ADDC A, Rn	Add register to accumulator with carry
ADDC A, direct	Add directly addressed data to accumulator with carry
ADDC A, @Ri	Add indirectly addressed data to accumulator with carry
ADDC A, #data	Add immediate data to accumulator with carry
SUBB A, Rn	Subtract register from accumulator with borrow
SUBB A, direct	Subtract directly addressed data from accumulator with borrow
SUBB A, @Ri	Subtract indirectly addressed data from accumulator with borrow
SUBB A, #data	Subtract immediate data from accumulator with borrow
INC A	Increment accumulator
INC Rn	Increment register
INC direct	Increment directly addressed location
INC @Ri	Increment indirectly addressed location
INC DPTR	Increment data pointer
DEC A	Decrement accumulator
DEC Rn	Decrement register
DEC direct	Decrement directly addressed location
DEC @Ri	Decrement indirectly addressed location
MUL AB	Multiply A and B
DIV	Divide A by B
DA A	Decimally adjust accumulator

Logic operations

Mnemonic	Description
ANL A, Rn	AND register to accumulator
ANL A, direct	AND directly addressed data to accumulator
ANL A, @Ri	AND indirectly addressed data to accumulator
ANL A, #data	AND immediate data to accumulator
ANL direct, A	AND accumulator to directly addressed location
ANL direct, #data	AND immediate data to directly addressed location
ORL A, Rn	OR register to accumulator

ORL A, direct	OR directly addressed data to accumulator
ORL A, @Ri	OR indirectly addressed data to accumulator
ORL A, #data	OR immediate data to accumulator
ORL direct, A	OR accumulator to directly addressed location
ORL direct, #data	OR immediate data to directly addressed location
XRL A, Rn	Exclusive OR (XOR) register to accumulator
XRL A, direct	XOR directly addressed data to accumulator
XRL A, @Ri	XOR indirectly addressed data to accumulator
XRL A, #data	XOR immediate data to accumulator
XRL direct, A	XOR accumulator to directly addressed location
XRL direct, #data	XOR immediate data to directly addressed location
CLR A	Clear accumulator
CPL A	Complement accumulator
RL A	Rotate accumulator left
RLC A	Rotate accumulator left through carry
RR A	Rotate accumulator right
RRC A	Rotate accumulator right through carry
SWAP A	Swap nibbles within the accumulator

Data transfer operations

Mnemonic	Description
MOV A, Rn	Move register to accumulator
MOV A, direct	Move directly addressed data to accumulator
MOV A, @Ri	Move indirectly addressed data to accumulator
MOV A, #data	Move immediate data to accumulator
MOV Rn, A	Move accumulator to register
MOV Rn, direct	Move directly addressed data to register
MOV Rn, #data	Move immediate data to register
MOV direct, A	Move accumulator to direct
MOV direct, Rn	Move register to direct
MOV direct1, direct2	Move directly addressed data to directly addressed location
MOV direct, @Ri	Move indirectly addressed data to directly addressed location
MOV direct, #data	Move immediate data to directly addressed location
MOV @Ri, A	Move accumulator to indirectly addressed location
MOV @Ri, direct	Move directly addressed data to indirectly addressed location

MOV @Ri, #data	Move immediate data to in directly addressed location
MOV DPTR, #data16	Load data pointer with a 16-bit immediate
MOVC A, @A+DPTR	Load accumulator with a code byte relative to DPTR
MOVC A, @A+PC	Load accumulator with a code byte relative to PC
MOVX A, @Ri	Move external RAM (8-bit address) to accumulator
MOVX A, @DPTR	Move external RAM (16-bit address) to accumulator
MOVX @Ri, A	Move accumulator to external RAM (8-bit address)
MOVX @DPTR, A	Move accumulator to external RAM (16-bit address)
PUSH direct	Push directly addressed data onto stack
POP direct	Pop directly addressed location from stack
XCH A, Rn	Exchange register with accumulator
XCH A, direct	Exchange directly addressed location with accumulator
XCH A, @Ri	Exchange indirect RAM with accumulator
XCHD A, @Ri	Exchange low-order nibbles of indirect and accumulator

Boolean manipulation

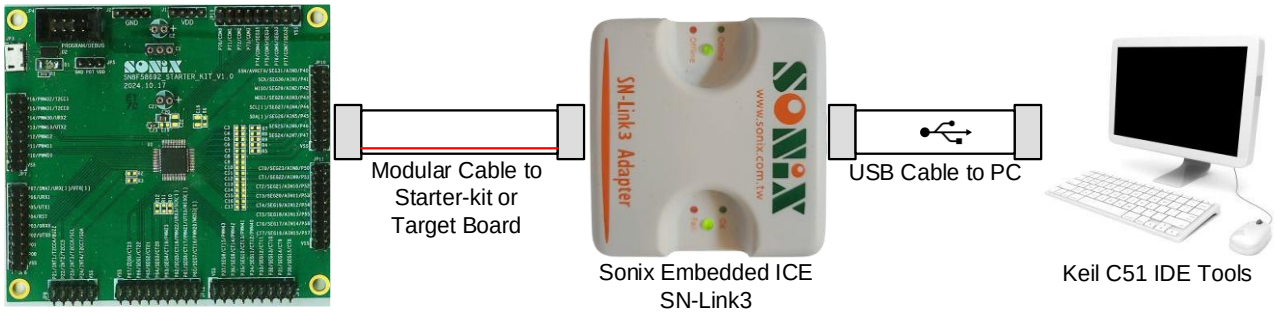
Mnemonic	Description
CLR C	Clear carry flag
CLR bit	Clear directly addressed bit
SETB C	Set carry flag
SETB bit	Set directly addressed bit
CPL C	Complement carry flag
CPL bit	Complement directly addressed bit
ANL C, bit	AND directly addressed bit to carry flag
ANL C, /bit	AND complement of directly addressed bit to carry
ORL C, bit	OR directly addressed bit to carry flag
ORL C, /bit	OR complement of directly addressed bit to carry
MOV C, bit	Move directly addressed bit to carry flag
MOV bit, C	Move carry flag to directly addressed bit

Program branches

Mnemonic	Description
ACALL addr11	Absolute subroutine call
LCALL addr16	Long subroutine call
RET	Return from subroutine
RETI	Return from interrupt
AJMP addr11	Absolute jump
LJMP addr16	Long jump
SJMP rel	Short jump (relative address)
JMP @A+DPTR	Jump indirect relative to the DPTR
JZ rel	Jump if accumulator is zero
JNZ rel	Jump if accumulator is not zero
JC rel	Jump if carry flag is set
JNC rel	Jump if carry flag is not set
JB bit, rel	Jump if directly addressed bit is set
JNB bit, rel	Jump if directly addressed bit is not set
JBC bit, rel	Jump if directly addressed bit is set and clear bit
CJNE A, direct, rel	Compare directly addressed data to accumulator and jump if not equal
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal
DJNZ Rn, rel	Decrement register and jump if not zero
DJNZ direct, rel	Decrement directly addressed location and jump if not zero
NOP	No operation for one cycle

34 Development Environment

SONIX provides an Embedded ICE emulator system to offer SN8F5869 firmware development. The platform is an in-circuit debugger and controlled by Keil C51 IDE software on Microsoft Windows platform. The platform includes SN-Link3, SN8F5869 Starter-kit and Keil C51 IDE software to build a high-speed, low cost, powerful and multi-task development environment including emulator, debugger and programmer. To execute emulation is like run real chip because the emulator circuit integrated in SN8F5869 to offer a real development environment.



34.1 Minimum Requirement

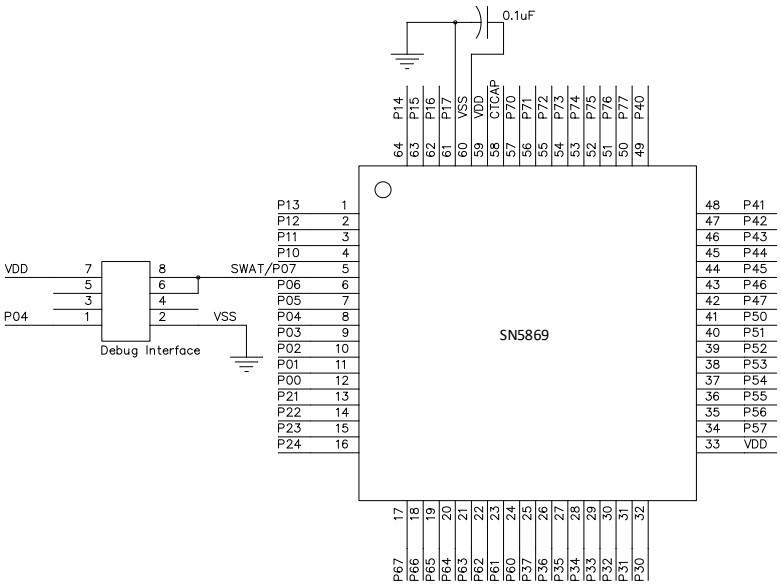
The following items are essential to build up an appropriate development environment. The compatibility is verified on listed versions, and is expected to execute perfectly on later version. SN-Link firmware and software updates and all the latest documentation can be downloaded from the Sonix support webpage at SONiX website (https://www.sonix.com.tw/article-en-3979-26453);
Keil C51 is downloadable on https://www.keil.com/download/product/ .

- **SN-Link3 Adapter**
- **SN-Link Driver for Keil C51**
- **Keil C51** version 9.50a or later.

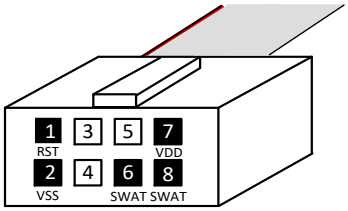
34.2 Debug Interface Hardware

The circuit below demonstrates the appropriate method to connect microcontroller's SWAT pin and SN-Link3 Adapter.

Before starting debug, microcontroller's power (VDD) must be switched off. Connect the SWAT to both 6th and 8th pins of SN-Link, and respectively link VDD and VSS to 7th pin and 2nd pin. A handshake procedure would be automatically started by turn on the microcontroller, and SN-Link's green LED (Run) indicates the success of connection.



example circuit

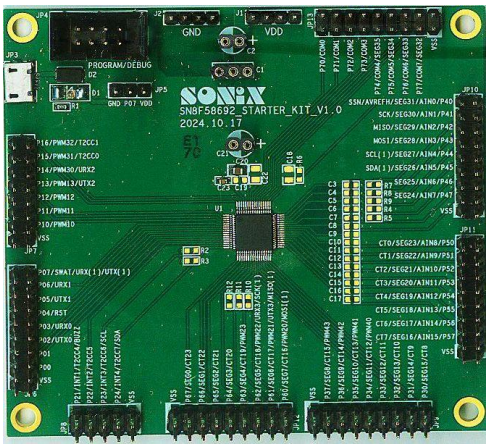


SN-Link header

34.3 Development Tool

SN-Link3 Adapter

Starter-Kit support SN8F58692



MP5 Writer

35 SN8F5869 Starter-Kit

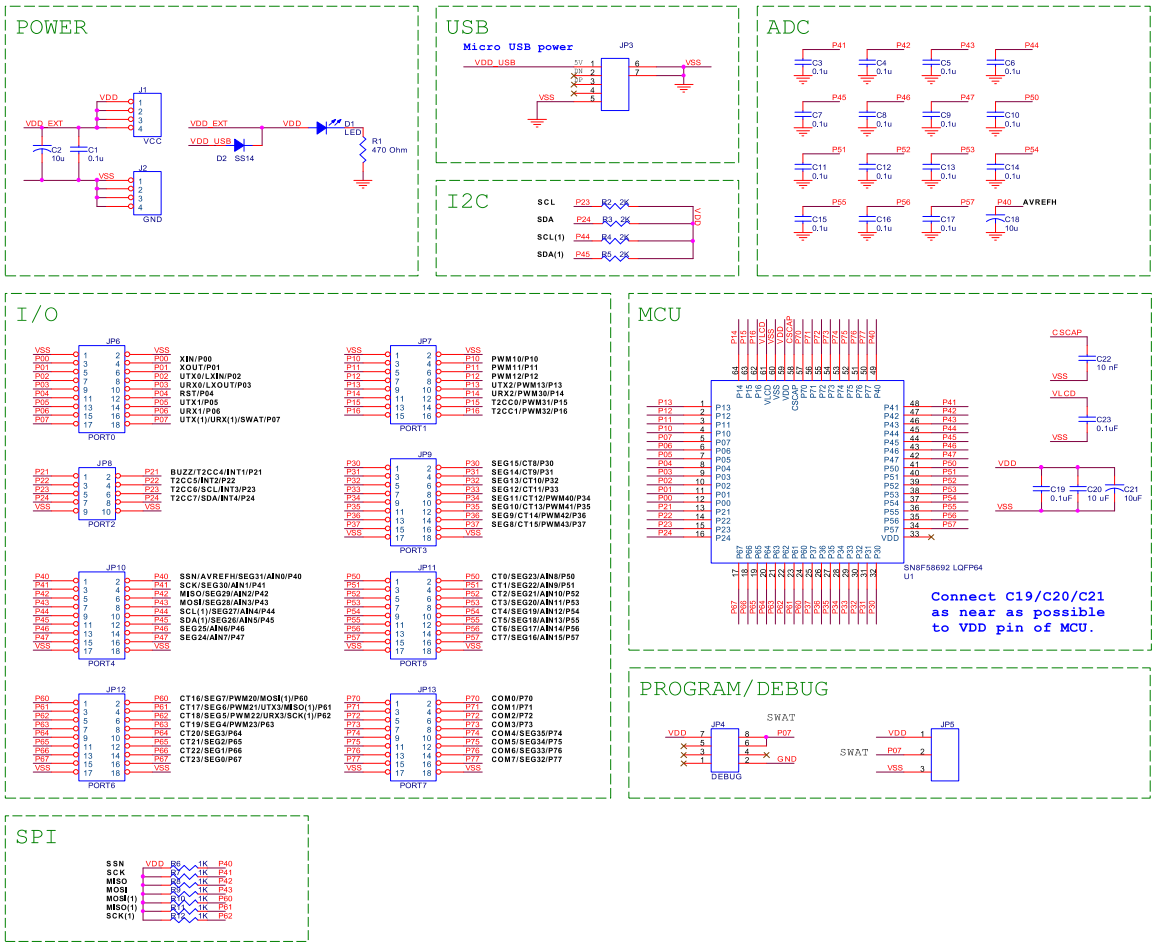
SN8F5000 Starter-Kit provides easy-development platform. It includes SN8F5000 family real chip and I/O connectors to input signal or drive device of user's application. It is a simple platform to develop application as target board not ready. The Starter-Kit can be replaced by target board, because SN8F5000 family integrates embedded ICE in-circuit debugger circuitry.

35.1 Configurations of Circuit

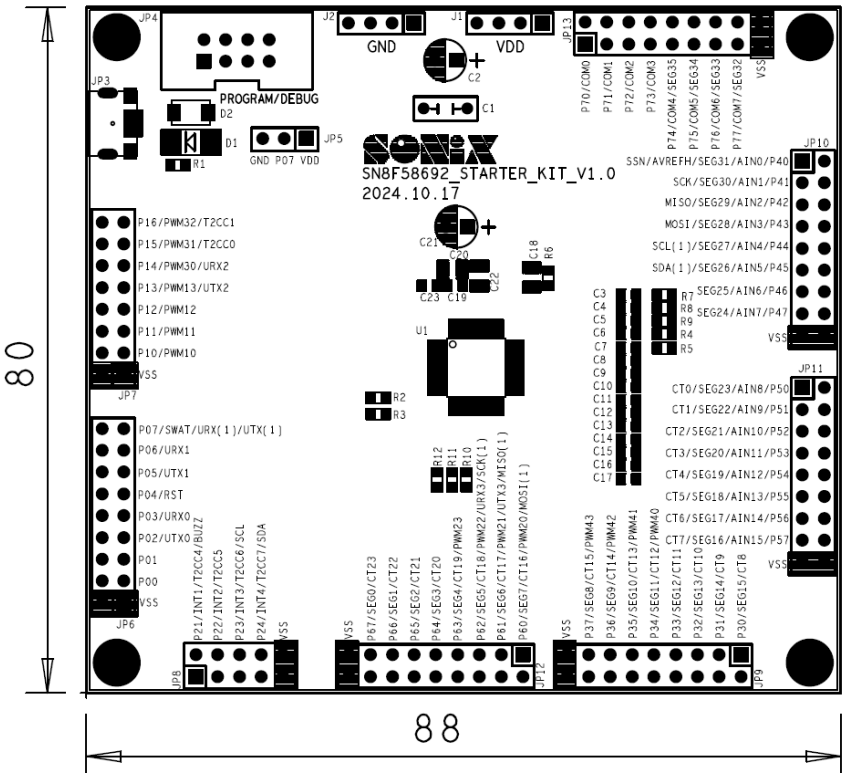
These configurations must be setup completely before starting Starter-Kit developing.

1. Confirm to the circuit board whether elements are complete.
2. The power source of Starter-Kit circuit is chosen from 5.0V, 3.3V, external power or Micro USB via jumper.
3. The power source comes from 5.0V or 3.3V which must be connect to DC 7.5V power adapter.
4. If the power source is chosen from external power, then external power source connects to EXT pin.
5. The "RST" pin needs to connect pull high resister to VDD when external reset is chosen to use.
6. The "XIN" pin and the "XOUT" pin need to connect crystal/resonator oscillator components when system clock is setting crystal or RTC mode.
7. The "XIN" pin needs to connect external clock source when system clock is setting external clock input mode.
8. The Debug Port can connect SN-LINK Adapter for emulation or download code.
9. The MCU LED will light up and SN8F5000 family chip will be connected to power when power (VDD) is switched on.

35.2 Schematic



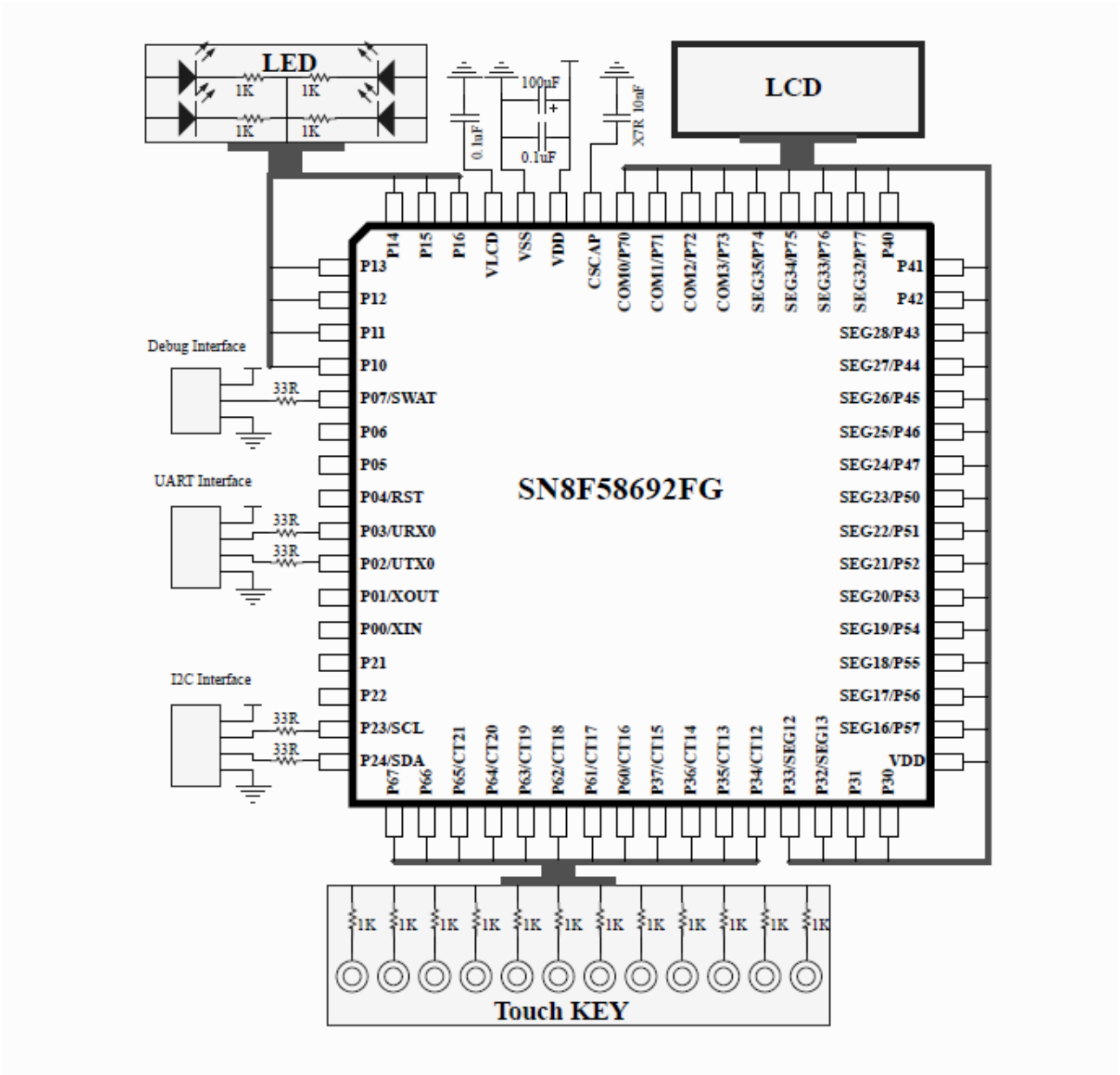
35.3 Floor Plan of PCB layout



35.4 Component Description

Number	Description
C3 – C17	ADC channel capacitors
C18	AVREFH capacitor
C1/C2	Power VDD capacitors
C19-C21	MCU VDD capacitors
C22	CSCAP capacitor
C23	VLCD capacitor
D1	MCU direct LED
J1/J2	External power source
JP3	Micro USB port, VDD power source from USB 5V
JP4	Debug Port
JP6 – JP13	I/O connector
R2 – R12	I2C and SPI Interface pull-high resisters
U1	SN8F58692F real chip (Sonix standard option)

36 Application Circuit



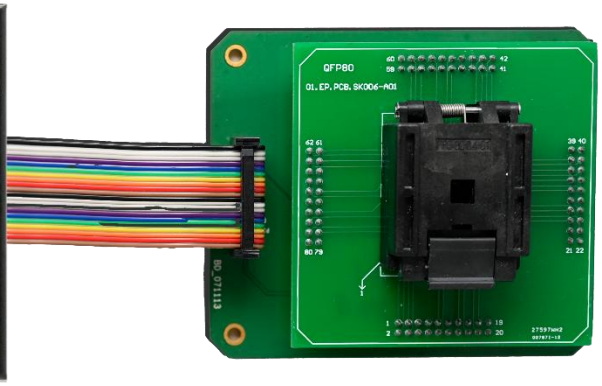
37 ROM Programming Pin

SN8F5869 Series Flash ROM erase/program/verify support SN-Link and MP5 Writer

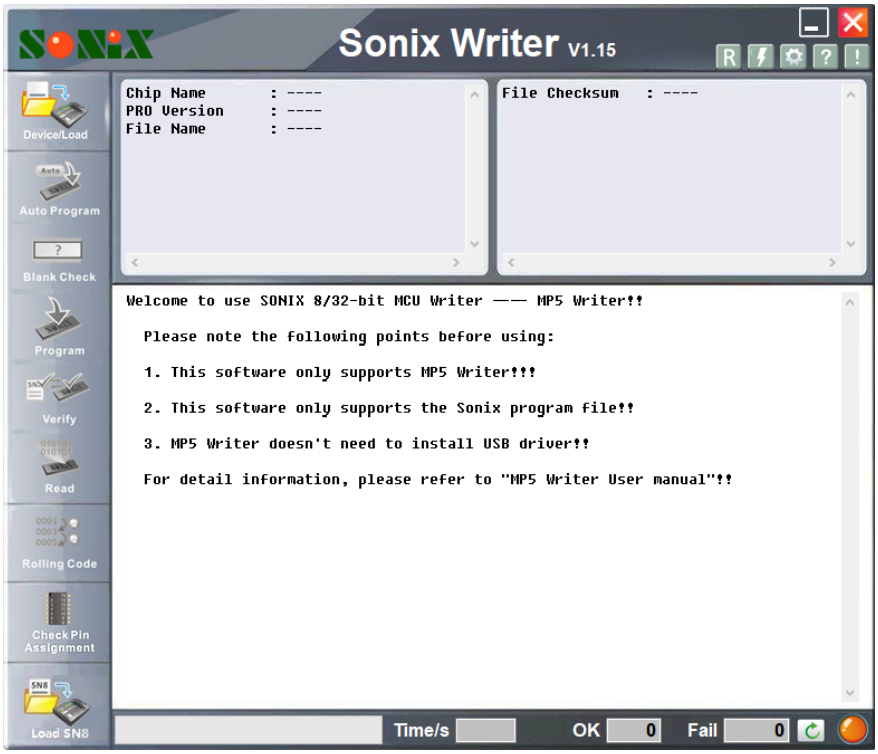
- SN-Link: Debug interface and on board programming.
- MP5 Writer: For SN8F5869 series version mass programming.

37.1 MP5 Hardware Connecting

Different package type with MCU programming connecting is as following.



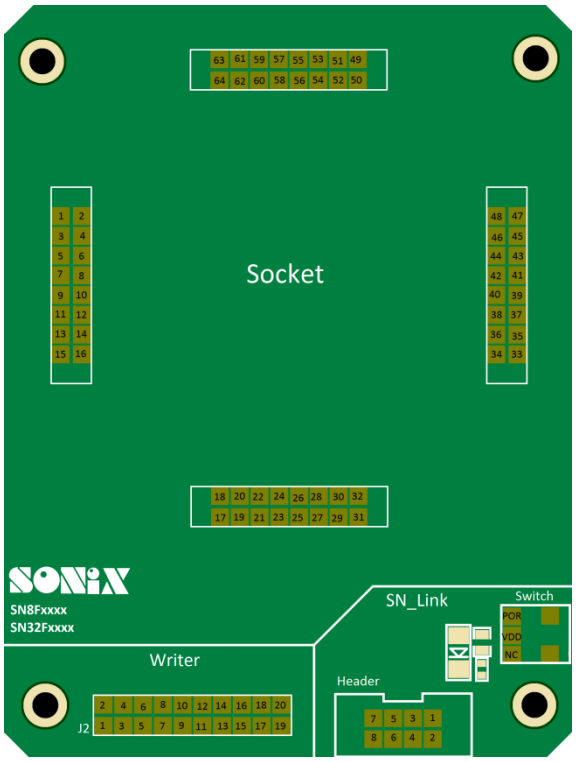
MP5 Software operation interface is as following.



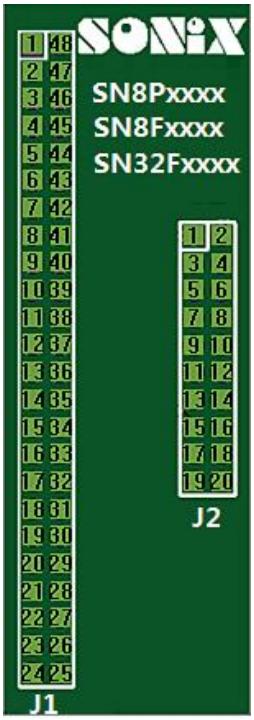
37.2 MP5 Writer Transition Board Socket Pin Assignment

MP5 Writer Transition Board:

For 64 pins



For less than or equal to 48 pins



37.3 MP5 Writer Programming Pin Mapping

MP5 Writer programming pins as following.

Writer Connector		MCU Pin Name	SN8F58692F		SN8F58682F	
J2 Pin Number	J2 Pin Name		MCU Pin Number	J1 Pin Number	MCU Pin Number	J1 Pin Number
1	VDD	VDD	59	-	43	43
2	GND	VSS	60	-	44	44
7, 9	SWAT	P0.7	5	-	3	3
20	PDB	P0.1	11	-	7	7

Writer Connector		MCU Pin Name	SN8F58652F/J		SN8F58641S/T		SN8F58631X	
J2 Pin Number	J2 Pin Name		MCU Pin Number	J1 Pin Number	MCU Pin Number	J1 Pin Number	MCU Pin Number	J1 Pin Number
1	VDD	VDD	29	37	28	38	24	36
2	GND	VSS	30	38	1	11	1	13
7, 9	SWAT	P0.7	32	40	2	12	2	4
20	PDB	P0.1	4	12	3	13	3	5

37.4 SN-Link ICP Programming

SN-Link ICP programming hardware and software are as following.

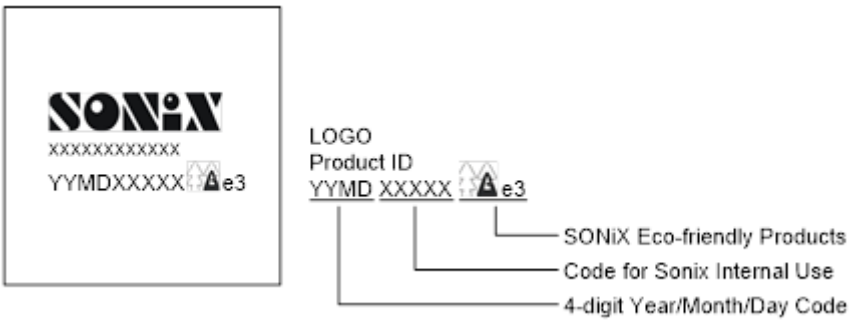
37.5 SN-Link ICP Programming Pin Mapping

SN-Link Connector		MCU Pin Name	SN8F58692F	SN8F58682F
Pin Number	Pin Name		Pin Number	Pin Number
7	VDD	VDD	59	43
2	GND	VSS	60	44
6, 8	SWAT	P0.7	5	3

SN-Link Connector		MCU Pin Name	SN8F58652F/J	SN8F58641S/T	SN8F58631X
Pin Number	Pin Name		Pin Number	Pin Number	Pin Number
7	VDD	VDD	29	28	24
2	GND	VSS	30	1	1
6, 8	SWAT	P0.7	32	2	2

38 Ordering Information

The figure below is an example of the marking. Contents such as the product ID or symbol may vary according to different packages.

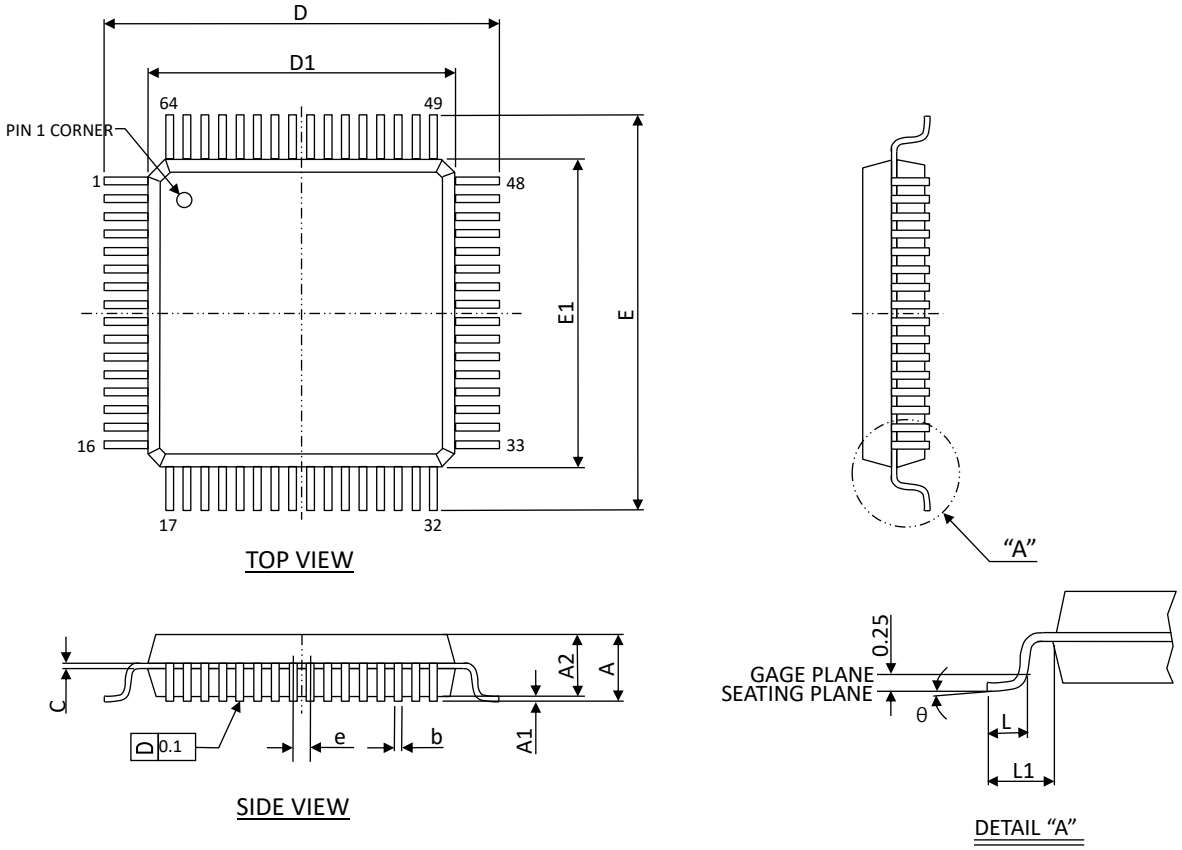


38.1 Device Nomenclature

Full Name	Packing Type
S8F5869W	Wafer
SN8F5869H	Dice
SN8F58692FG	LQFP, 64 pins, Green package
SN8F58682FG	LQFP, 48 pins, Green package
SN8F58652FG	LQFP, 32 pins, Green package
SN8F58652JG	QFN, 32 pins, Green package
SN8F58641SG	SOP, 28 pins, Green package
SN8F58641TG	TSSOP, 28 pins, Green package
SN8F58631XG	SSOP, 24 pins, Green package

39 Package Information

39.1 LQFP64 7x7

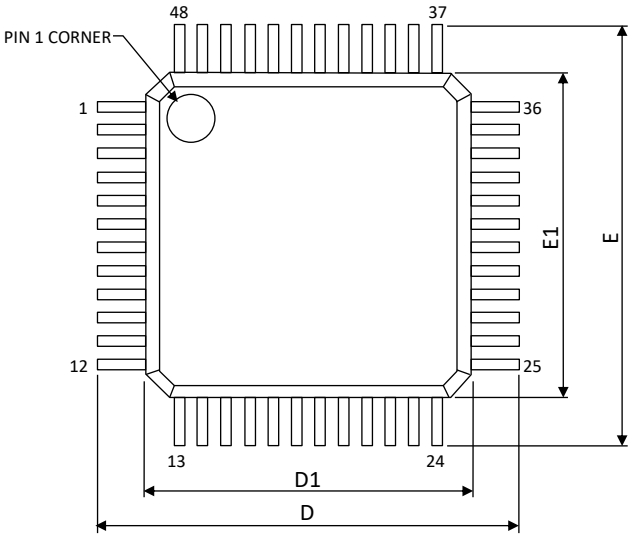


SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.25	0.002	--	0.01
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.19	0.25	0.005	0.007	0.010
c	0.09	--	0.20	0.004	--	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
L	0.4	0.60	0.8	0.016	0.024	0.032
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

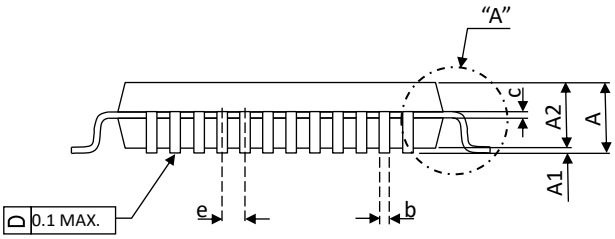
Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

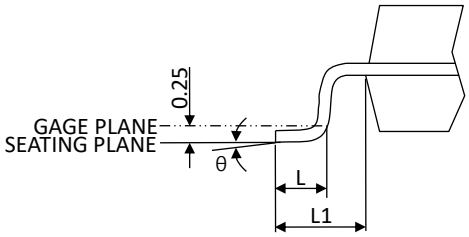
39.2 LQFP48 7x7



TOP VIEW



SIDE VIEW



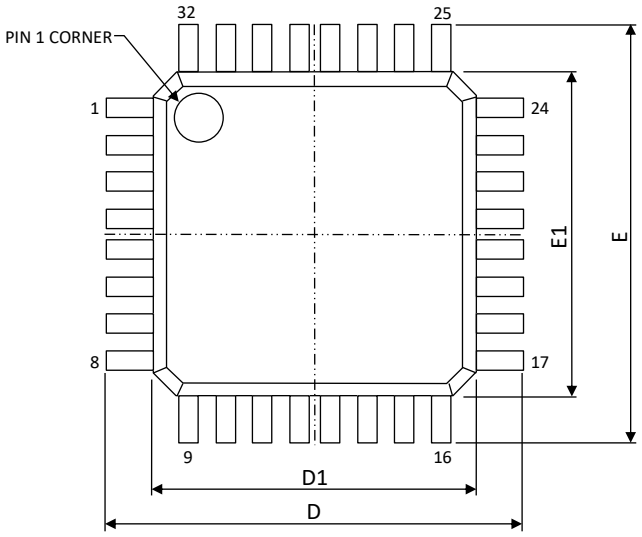
DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.15	0.002	--	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	--	0.20	0.004	--	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

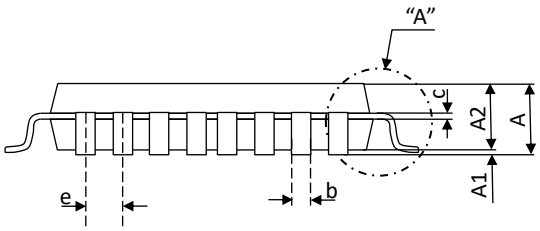
Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

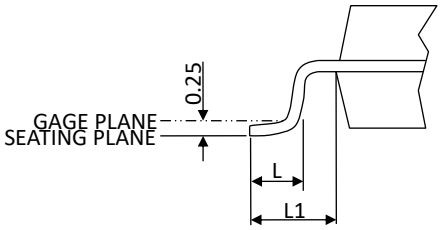
39.3 LQFP32 7x7



TOP VIEW



SIDE VIEW



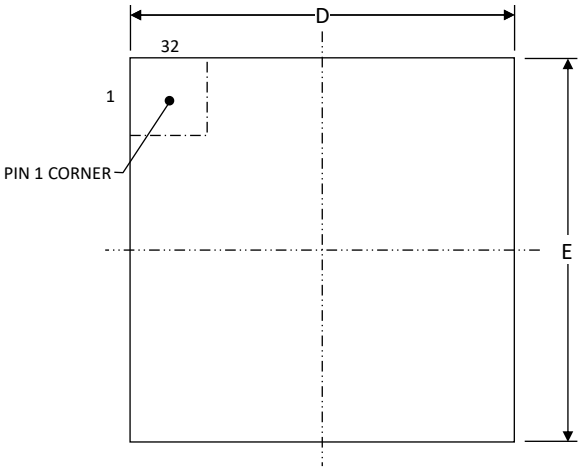
DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.25	0.002	--	0.01
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	--	0.45	0.012	--	0.018
c	0.09	--	0.20	0.004	--	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.80 BSC			0.031 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	1.00 REF			0.039 REF		

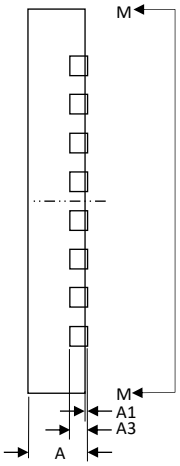
Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

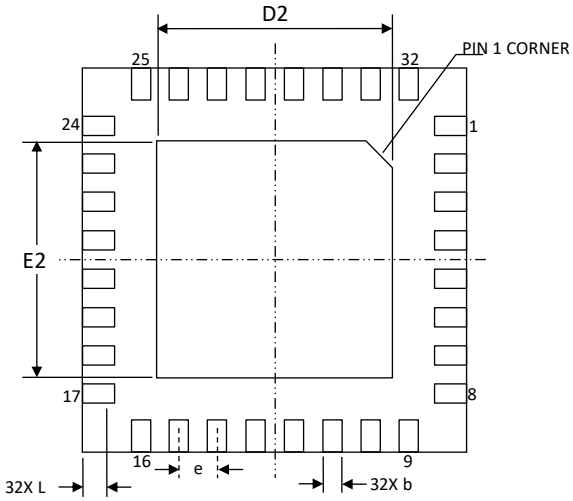
39.4 QFN32 4x4



TOP VIEW



SIDE VIEW



BOTTOM VIEW

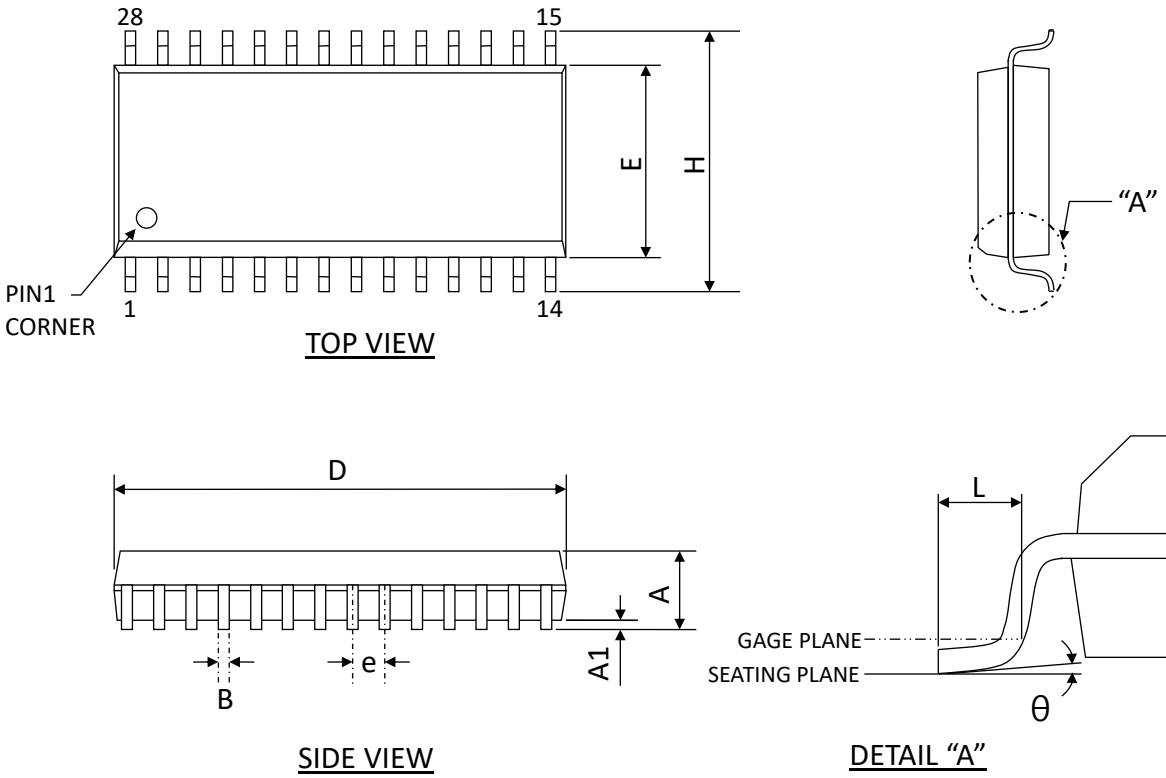
VIEW M - M

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.000	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D		4.00 BSC			0.157 BSC	
E		4.00 BSC			0.157 BSC	
e		0.40 BSC			0.016 BSC	
D2	2.00	2.45	2.90	0.080	0.096	0.114
E2	2.00	2.45	2.90	0.080	0.096	0.114
L	0.25	0.35	0.45	0.010	0.013	0.017

Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)

39.5 SOP28

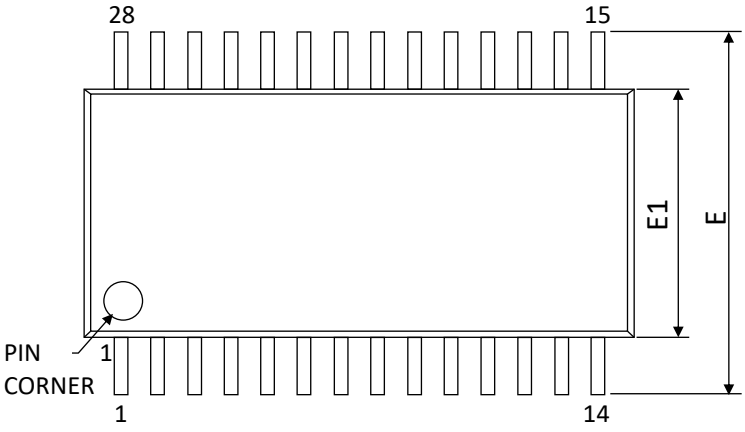


SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	2.65	--	--	0.104
A1	0.10	--	0.30	0.004	--	0.011
B	0.31	0.41	0.51	0.012	0.016	0.020
D	17.70	18.20	18.70	0.697	0.716	0.736
E	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
H	10.30 BSC			405 BSC		
L	0.40	--	1.27	0.016	--	0.050
θ	0°	4 °	8°	0°	4 °	8°

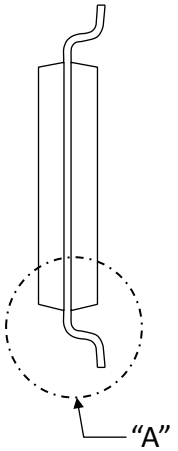
Notes：

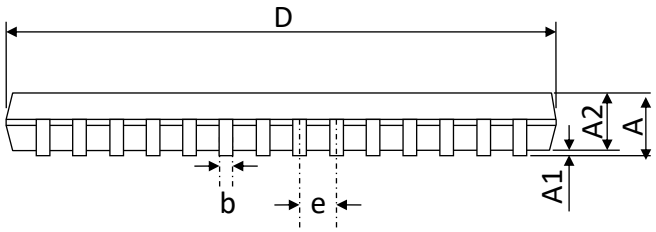
1. CONTROLLING DIMENSION：mm
2. JEDEC OUTLINE : MO-119 AB

39.6 TSSOP28

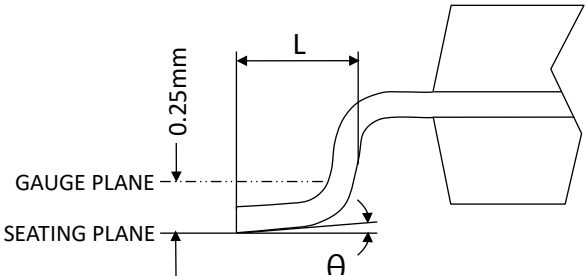


TOP VIEW





SIDE VIEW



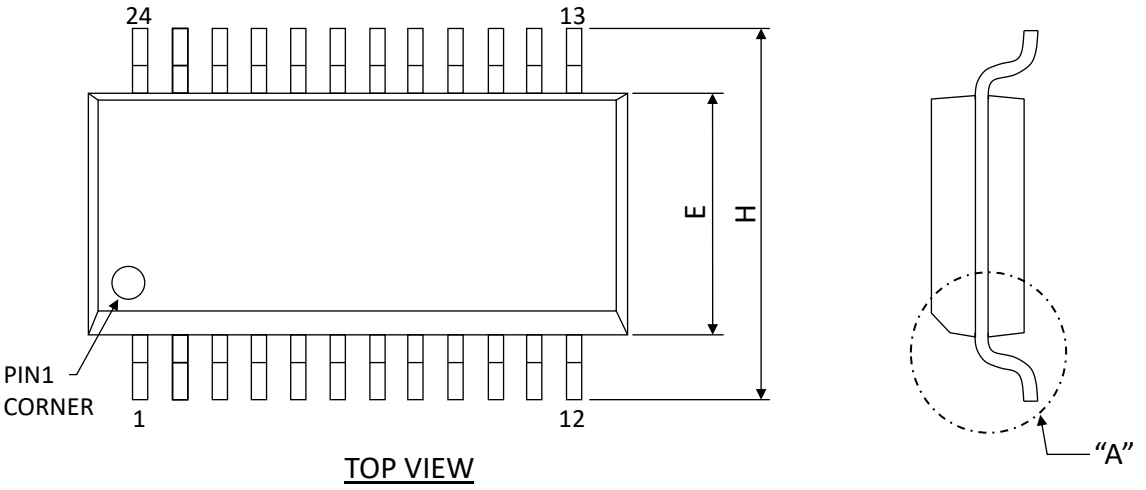
DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.20	--	--	0.047
A1	0.00	--	0.15	0.000	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
D	9.60	9.70	9.80	0.378	0.382	0.386
E	6.40 BSC.			0.252 BSC.		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC.			0.026 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	--	8°	0°	--	8°

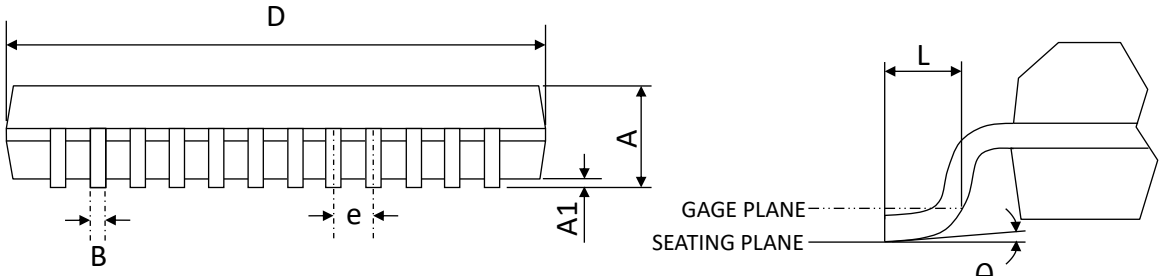
Notes：

1. CONTROLLING DIMENSION：mm
2. JEDEC OUTLINE : MO-153
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BERRES.
4. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION.

39.7 SSOP24



TOP VIEW



SIDE VIEW

DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.75	--	--	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
B	0.20	--	0.30	0.008	--	0.012
D	8.55	8.65	8.75	0.337	0.341	0.344
E	3.80	3.90	4.0	0.150	0.154	0.157
e	0.635 BSC.			0.025 BSC.		
H	5.80	6.00	6.20	0.228	0.236	0.244
L	0.41	0.64	1.27	0.016	0.025	0.050
θ	0°	--	8°	0°	--	8°

Notes：

1. CONTROLLING DIMENSION：INCH
2. JEDEC OUTLINE : MO-137 AE

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